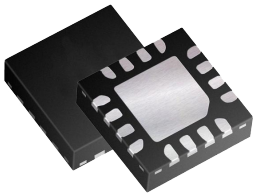
EPC C1G2 COMPLIANT UHF RFID TAG WITH POWER HARVESTING AND SPI COMMUNICATION FOR EXTERNAL LOW POWER SENSORS AND ACTUATORS

Check for samples: ROCKY100



FEATURES

- 860MHz-960MHz operation
- EPC C1G2 compliant
- ISO 18000-6 Type C compliant
- 160-bit EPC Bank: Up to 128-bit EPC
- 96-bit TID Bank: Up to 48-bit Serial Number
- Partitioned User Bank: Up to 1008-bit Non Volatile User Data
- Password protected *Kill* command
- Password protected *Access* command
- Forward link data rates: 26.7kbps to 128 kbps
- Return link data rates: 40 to 640 kbps
- Return link modulations: FM0 and Miller subcarrier (2, 4, 8)
- Read sensitivity in passive mode without sensors: -14dBm
- High sensitivity in passive mode supplying external sensors: -10dBm (typical case)
- Configurable sensitivity for battery assisted mode: -24dBm (BAP) or -35dBm (EBAP)
- Configurable PSK modulation depth
- Configurable regulated output from 1.2V to 3.0V
- VDD monitor and configurable control for activation of load supply
- Battery switch with 500nA leakage current in open state
- 5 configurable GPIOs
- Configurable SPI master module to control external devices
- SPI slave module to access C1G2 memory space
- Edge detector for anti-tampering
- Event logger with timestamp
- PWM output generator
- C1G2 related event generator
- Front-end signal bypass
- Extended temperature range: -40°C to +85°C
- 4x4mm QFN-16 package

APPLICATIONS

- Wireless identification
- Energy harvesting
- Batteryless wireless sensors/actuators
- TPMS (Tire Pressure Monitoring Systems)
- Cold chain monitoring
- Orientation monitoring
- Fill level monitoring
- Open/close detection

CONTENTS

DEVICE OVERVIEW

DESCRIPTION

ROCKY100 is an EPC Class-1 Generation-2 (C1G2) RFID tag IC which is compliant with ISO/IEC 18000-6 Type C. The chip offers advanced capabilities leading to a performance beyond that of standard RFID tags by including sensor measurements and actuator control.

The IC operates in a fully passive mode harvesting energy from the RF beam emitted by the reader. With an external power source, the IC can operate in Battery Assisted Passive (BAP) mode with enhanced communication range.

ROCKY100 includes a non volatile memory to store unique identifiers and passwords for item identification and data protection operations. The memory includes an up to 128-bit length *Electronic Product Code* (EPC) supporting EPCGlobal Tag Data Standards. The memory also includes a 96-bit length *Tag IDentifier* (TID) supporting ISO/IEC 15963 class-identification. Separate 32-bit length Kill and Access passwords are also included supporting protected kill and data access operations.

Additionally, ROCKY100 supports extending the classic functionality of C1G2 tags by attaching an external system to the IC. ROCKY100 includes the necessary power supply management circuitry to supply external sensors or actuators with the energy harvested from the RF field. It also includes configurable GPIOs to communicate with the external device, trigger operations and retrieve data prior to backscattering the obtained answer to the reader. All the operations are commanded by the reader using standard memory access commands making the system directly compatible with any standard C1G2 RFID system.

FUNCTIONAL BLOCK DIAGRAM

The functional block diagram of ROCKY100 is shown in figure 1. The RF front-end provides the core RFID functionality, including energy harvesting from the RF field, demodulation of *Amplitude Shift Keying* (ASK) symbols in the forward link and *Phase Shift Keying* (PSK) modulation of the impedance of the IC to backscatter data through the reverse link. The device allows configuring the ASK sensitivity and the PSK modulation depth.

The harvested energy is managed by a power supply management unit. This unit includes several low dropout regulators to provide stable supply voltages for internal circuitry and external devices. Several voltage monitors are included to ensure proper start-up of the system.

Additionally, the device can be powered up using an external battery. A dedicated pin allows connecting such a battery with low drain current and activating the use of the battery upon request.

A configurable LDO regulator is included for the load power supply generation. Moreover, the supply and ground of the load can be connected and disconnected automatically to ensure proper supply during the operation of the load by means of analog switches and a voltage monitor.

An application specific digital processor handles the ISO/IEC 18000-6 Type C air protocol managing the non volatile memory according to the standard. The digital processor controls several devices to add functionality to ROCKY100: 5 GPIOs, an SPI module (master/slave), an event generator, an edge detector, an event logger, a PWM generator and a signal bypass module.

The GPIOs can be used either as general purpose input/output, or can be configured to be controlled by the other peripherals.

The SPI module can be configured as a master or a slave device, and it can be used to control and retrieve data from external digital systems. In master mode, the operation of the SPI is commanded through standard memory access commands included in the ISO/IEC 18000-6 Type C standard.

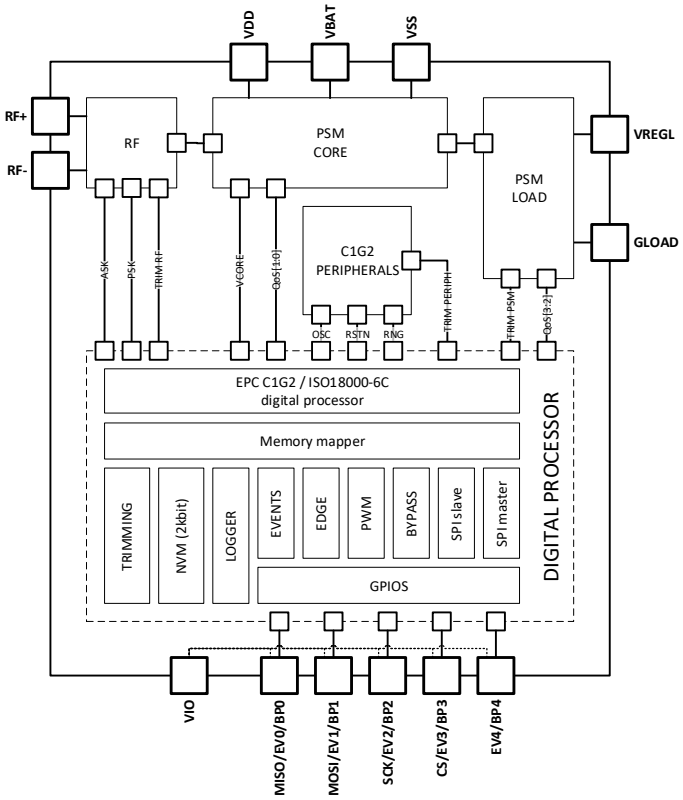


Figure 1: Block diagram of ROCKY100

The event generator allows notifying an external system when certain C1G2 relative event occurs. This functionality can be used to wake up external devices in a controlled way using UHF RFID readers.

The edge detector allows detecting state changes in input signals and adds anti-debounce capabilities.

The event logger keeps track of time and automatically logs timestamps and associated data values upon certain events, such as edge detection.

The PWM generator can be configured to generate a specific PWM signaling upon request.

The signal bypass module allows bypassing some of the internal signals provided by the RF front-end directly to the GPIOs. This mode is useful to use the physical layer of the EPC C1G2 standard and customize the upper layers. Note that in this case, the capability of communicating with commercial readers is no more controlled by the digital processor. The external device is responsible for fulfilling or not the communication standard.

Additionally, a configuration blockage system is implemented in order to allow blocking some of the configurable parameters.

TERMINAL CONFIGURATION AND FUNCTIONS

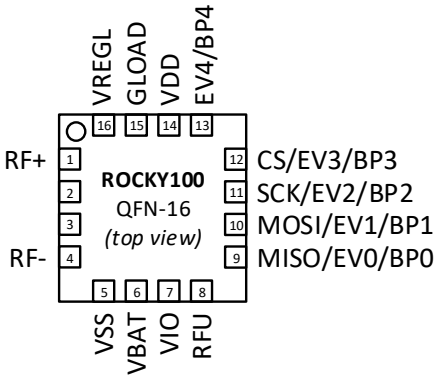


Figure 2: Pin diagram for QFN-16.

PIN		TYPE	DESCRIPTION
NAME	NO.		
RF			
RF+	1	RF	Positive input of differential RF signal
RF-	4	RF	Negative input of differential RF signal
Power supply			
VDD	14	Power	Supply voltage of the tag
VSS	5	Power	Ground of the tag
VBAT	6	Power	Battery supply voltage
VREGL	16	Power	Regulated load supply output
GLOAD	15	Power	Switched ground of the load
Digital I/O			
VIO	7	Power	Power supply for the digital I/O pins
RFU	8	Input	Reserved for future use. Connect to VSS.
MISO/EV0/BP0	9	I/O	SPI master input line / Event pin 0 / Bypass pin 0
MOSI/EV1/BP1	10	I/O	SPI master output line / Event pin 1 / Bypass pin 1
SCK/EV2/BP2	11	I/O	SPI clock line / Event pin 2 / Bypass pin 2
CS/EV3/BP3	12	I/O	SPI chip select line / Event pin 3 / Bypass pin 3
EV4/BP4	13	I/O	Event pin 4 / Bypass pin 4

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNIT
P_{RF}	RF input power		20	dBm
VDD	Supply voltage	-0.5	5.0	V
VIO	IO supply voltage	-0.5	5.0	V
v_{io}	Input voltage at any digital pin	-0.5	*VIO*+0.5	V
$T_{storage}$	Storage temperature	-40	125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
RF					
P_{RF}	RF input power			10	dBm
POWER SUPPLY					
VDD	Supply voltage	1.4		3.0	V
VBAT	Auxiliary supply voltage	1.4		3.0	V
VIO	IO supply voltage	1.4		3.0	V
TEMPERATURE					
$T_{operation}$	Operation temperature	-40		85	°C

NON VOLATILE MEMORY

PARAMETER	MIN	UNIT
Data retention @85°C	10	years
Number of erase/write cycles	10^4	cycles

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
RF						
RF_{SENS}	RF sensitivity ID			-14		dBm
	RF sensitivity Typical Load [1]			-10		dBm
	RF sensitivity BAP			-24		dBm
	RF sensitivity Enhanced BAP			-35		dBm
Z_{IN}	Input impedance ID	QF16@868MHz		64 - 469j		Ω
		QF16@915MHz		51 - 460j		Ω
	Input impedance Typical Load	QF16@868MHz		80 - 493j		Ω
		QF16@915MHz		52 - 479j		Ω
	Input impedance BAP	QF16@868MHz		35 - 451j		Ω
		QF16@915MHz		14 - 456j		Ω
TAG POWER SUPPLY						
VDD	Supply voltage		1.4	V_L	V_L+0.2	V
V_L	Limitation voltage			3.2		V
I_{DD}	Supply current	Base		7		μA
		Enhanced BAP		+2		μA
		VDD Monitor		+1		μA
		VREGL LDO		+0.5		μA
I_{BAT}	Battery leakage current[2]			0.5		μA
LOAD POWER SUPPLY						
$VREGL$	Regulated load supply output		1.2		3.0	V
RES_{VREGL}	Resolution of VREGL voltage				3	mV
ACC_{VREGL}	Accuracy of VREGL voltage			±5		%
I_{VREGL}	Driving strength of VREGL		0		5	mA
DIGITAL I/O						
VIO	IO supply voltage		1.4		3.6	V
V_{ih}	Input high voltage		0.7× VIO		VIO+0.5	V
V_{il}	Input low voltage		-0.5		0.3× VIO	V
I_{lkg}	Input leakage current				±1	μA
V_{oh}	Output high voltage		0.8× VIO			V
V_{ol}	Output low voltage				0.2× VIO	V
I_{drive}	Output driving strength [1]				1	mA

[1] Typical Load of 5 μA at 1.8V
[2] With BATSW in open state. When BATSW is closed, $I_{BAT} = I_{DD}$.

DETAILED DESCRIPTION

RF

The RF block can harvest energy from the incoming RF signal in the antenna. It has an integrated voltage multiplier in order to escalate the small AC voltage at the input of the antenna to a higher DC voltage. The voltage available in VDD will depend on the incoming RF energy and the load connected to the tag. The following figure shows the typical behavior of ROCKY100 for different load conditions.

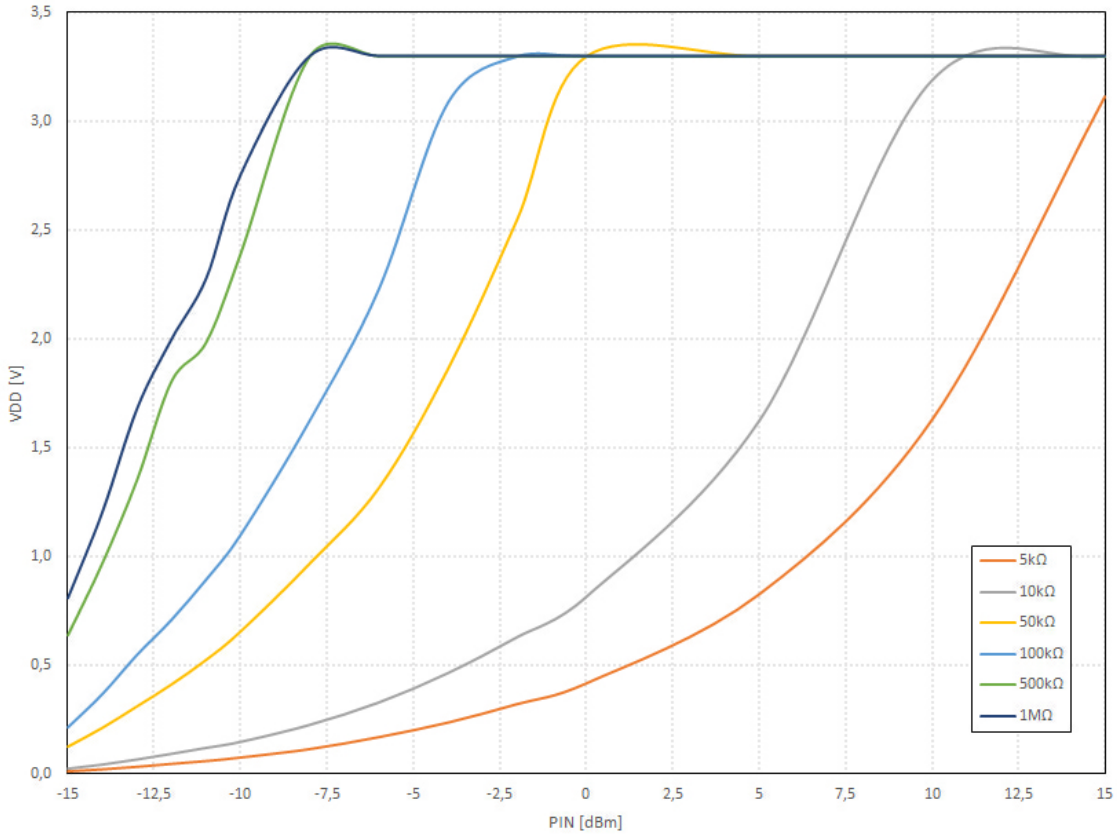


Figure 3: VDD (V) vs. P_{IN} (dBm) for different R_{LOAD}.

The RF block includes a voltage limiter to make sure that the voltage available at VDD never exceeds the limits of the technology. An external load can be connected to VDD to power external devices.

A battery can be connected to VDD so that the RF block is only used for passive communication. In this configuration, both the supply current of the RFID circuitry and the load are powered by the battery. Thus, the sensitivity of the tag is improved to the communication sensitivity. Moreover, in this configuration the high sensitivity demodulator can be enabled enhancing the communication sensitivity in expenses of increasing slightly the current consumption.

POWER SUPPLY MANAGEMENT

ROCKY100 includes a complete PSM for proper operation. In the one hand, this system manages the incoming energy from the RF front-end. This energy is delivered both to the internal circuitry and to the load of the device.

In the other hand, the system also controls a battery power input. If a power source is connected to this input, depending on the active configuration, the PSM will connect this input to the supply voltage of the device or keep it disconnected with a low leakage current.

Moreover, the PSM includes a smart control system to power up the external loads. For instance, a configurable LDO regulator is used to provide a stable voltage to the external load. Additionally, an analog switch can be used to connect the ground of the load to VSS only under certain circumstances. Finally, a voltage monitor is included to activate the LDO regulator and the ground switch when the supply voltage is within a configurable range.

POWER SIGNALS

For a clear understanding of the following description, a brief summary of the available power signals is presented:

- VDD: positive supply voltage of the device. The positive voltage generated in the RF energy harvester is delivered to this net.
- VSS: negative supply voltage of the device. The negative voltage generated in the RF energy harvester is delivered to this net.
- VBAT: battery input. This power signal can be connected to VDD changing the configuration bits.
- VREGL: configurable LDO regulator output for external loads. This block is powered from VDD.
- GLOAD: switched ground for external loads. The switching behavior is controlled with configuration bits.

VDD, VSS: MAIN POWER SUPPLY

The power nets VDD and VSS are the main power supply of ROCKY100. All internal electronics of the device drain their operating current from this source.

The RF energy harvesting module injects small amounts of current through a voltage multiplier to the supply capacitor connected to these nets. Thus, when the device is in presence of an RF emitter, some DC voltage will appear in VDD. As detailed in figure 3, the generated voltage depends on the input power in the RF pins and the average power consumption of the device.

The internal electronics of ROCKY100 are designed taking into account the nature of this power supply. However, even if it is possible to connect an external load to VDD, it is not recommended to do so. These loads have to comply several restrictions. First of all, the average power consumption of the external device must be low enough to be powered by the harvested energy. Additionally, as no regulation is applied to the main supply signals, the load has to support a variable supply voltage. Finally, the load can not have high current consumption peaks, as this would make the system oscillate during start-up. There are not many sensors nor actuators fulfilling all these conditions.

In order to make ROCKY100 an easy to use device, the PSM provides a regulated voltage supply to the external load. Moreover, the supply and ground of this load are switched off during start-up of the tag, so that they are connected only after monitoring a high enough supply voltage to assure a stable start-up.

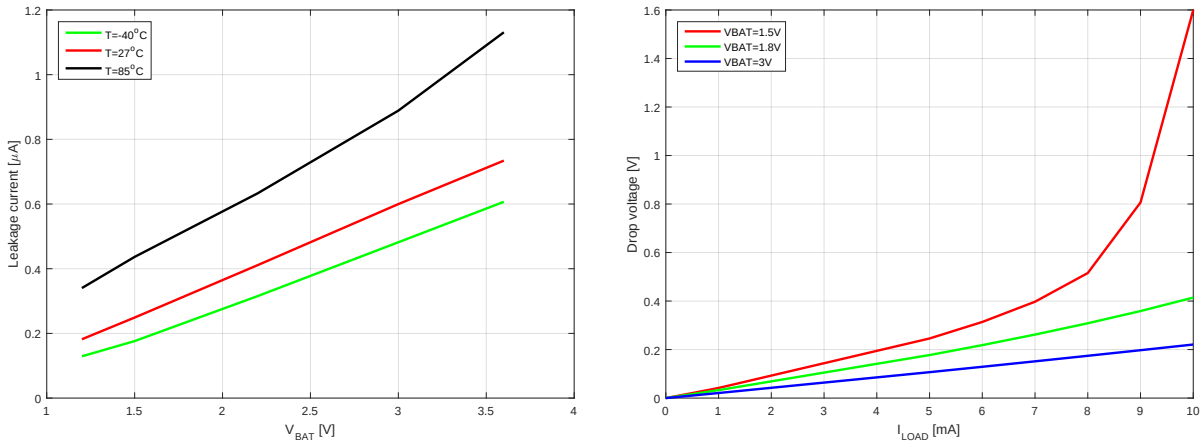
VBAT: AUXILIARY POWER SUPPLY

ROCKY100 can be used in BAP mode. This means that a battery can be used to enhance the characteristics of the device. However, in many applications it may be of interest to connect the battery without starting to drain

energy from it, and activate the current drain later on. This functionality allows manufacturing and assembling the final product with the battery, store it for some time without draining out the battery, and activate the use of the device wirelessly when required.

For that purpose the dedicated battery pin VBAT is included in ROCKY100. This net is not directly connected to VDD, but through a configurable analog switch. The state of the switch can be changed by means of the digital interfaces of the device, such as the RF or SPI interface.

The following graphs show the detailed characteristics of the VBAT switch.

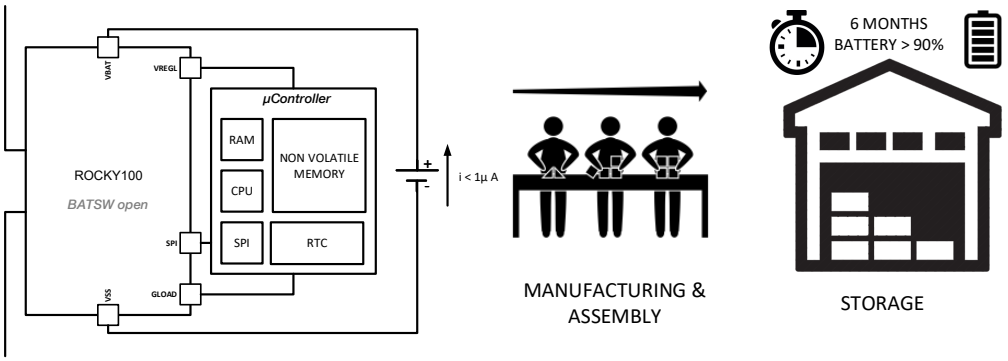


(a) Leakage current with battery switch off

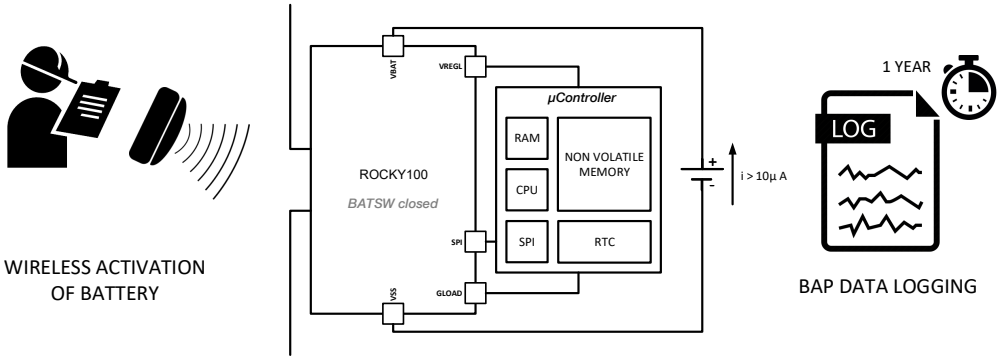
(b) Dropout voltage with battery switch on

Figure 4: Detailed characteristics of VBAT switch.

The next image shows an example usage of this functionality. First, a ROCKY100 powered BAP data logger is manufactured and assembled with a battery. The device is stored in a warehouse for 6 months. Then the product is taken to the field and the battery is activated via RF interface. In this step, the activation is done with passive characteristic as the battery has not been activated yet. Then, the device is used during 1 year logging sensor information with BAP characteristics.



(a) BAP datalogger in idle mode ($i_{DD} < 1\mu A$)



(b) BAP datalogger in active mode ($i_{DD} > 10\mu A$)

Figure 5: BAP datalogger example.

VREGL: REGULATED OUTPUT

ROCKY100 includes a low dropout regulator in the PSM block. The output voltage of this regulator can be configured inside the 1.2V-3.0V range. An integrated trimming resistor is used to configure the feedback value of the regulator. The output voltage of VREGL can be set modifying the TRIM_PSM register.

This regulator can be enabled and disabled automatically commanded by VDD MONITOR or can be manually controlled by the user (refer to section PSM in page 41 for further details). Make sure the VDD monitor is configured correctly prior to using the VREGL output in automatic switching mode.

The following graphs show the typical characteristics of the VREGL LDO regulator.

$T_J = 25°C$, $VDD = VREGL + 0.3V$, $I_{LOAD} = 10\mu A$ and $C_{LOAD} = 1nF$ unless otherwise noted.

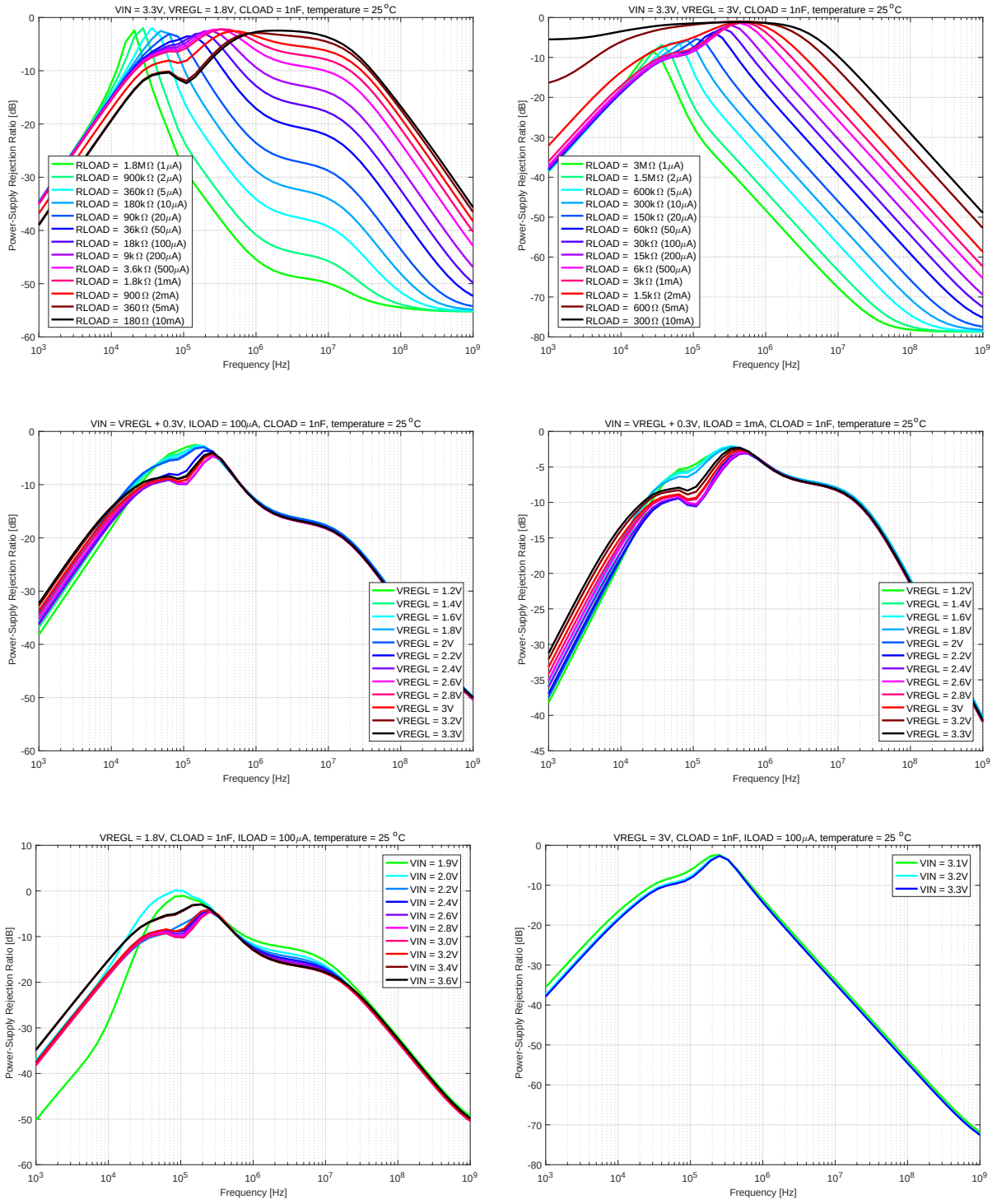


Figure 6: Typical characteristics of VREGL LDO regulator. (Part 1)

$T_J = 25°C$, $VDD = VREGL + 0.3V$, $I_{LOAD} = 10\mu A$ and $C_{LOAD} = 1nF$ unless otherwise noted.

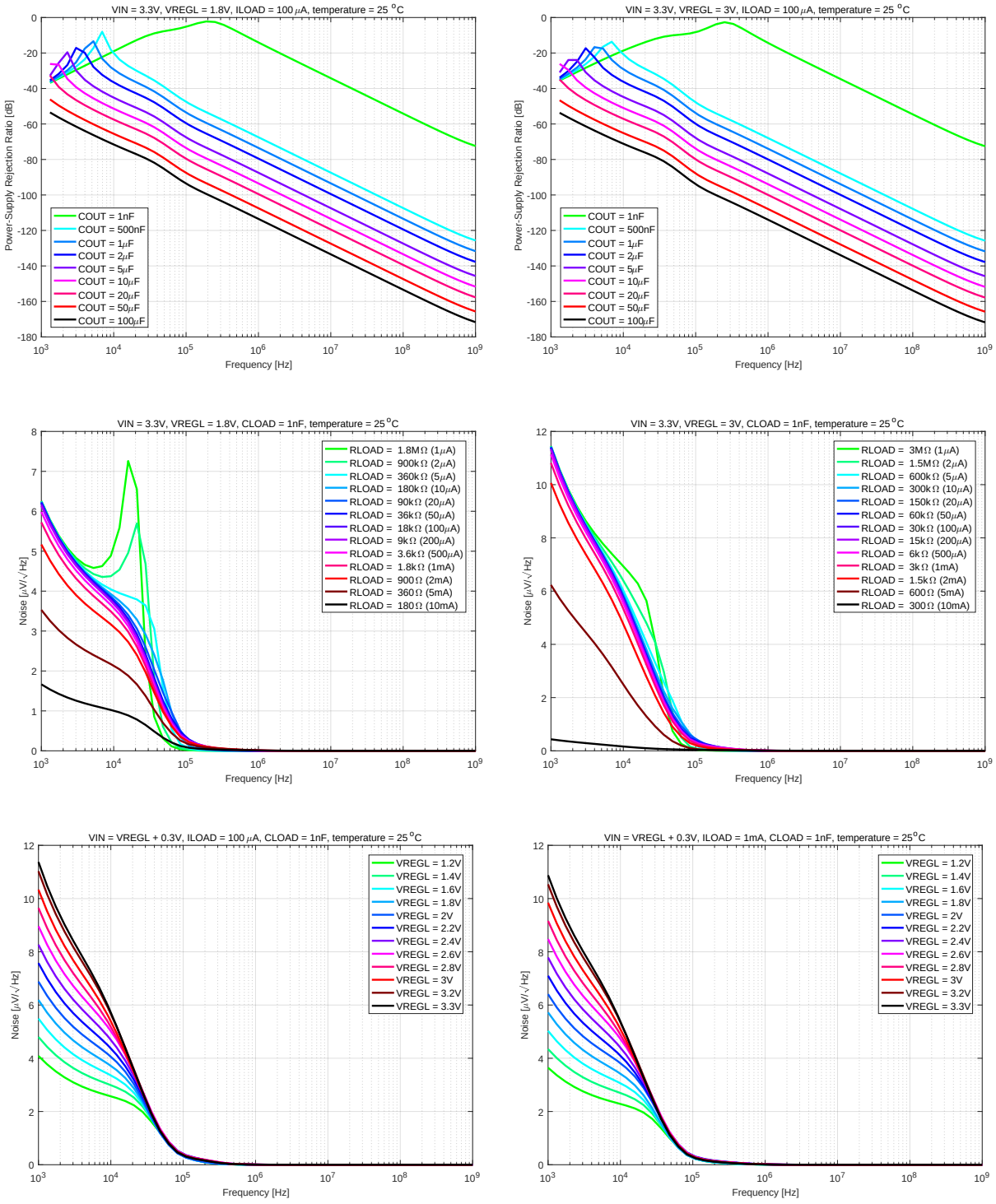


Figure 7: Typical characteristics of VREGL LDO regulator. (Part 2)

$T_J = 25°C$, $VDD = VREGL + 0.3V$, $I_{LOAD} = 10\mu A$ and $C_{LOAD} = 1nF$ unless otherwise noted.

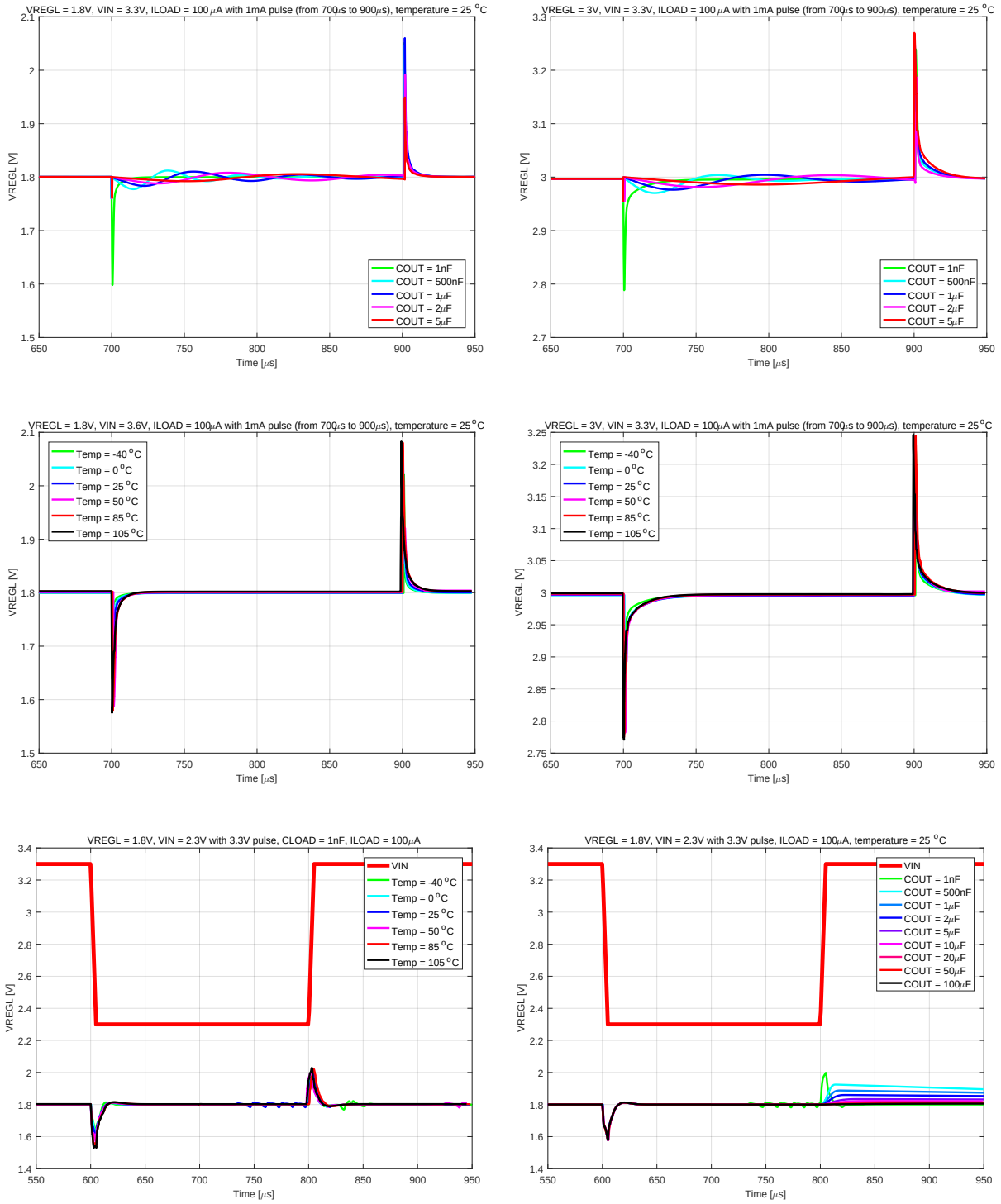


Figure 8: Typical characteristics of VREGL LDO regulator. (Part 3)

$T_J = 25°C$, $VDD = VREGL + 0.3V$, $I_{LOAD} = 10\mu A$ and $C_{LOAD} = 1nF$ unless otherwise noted.

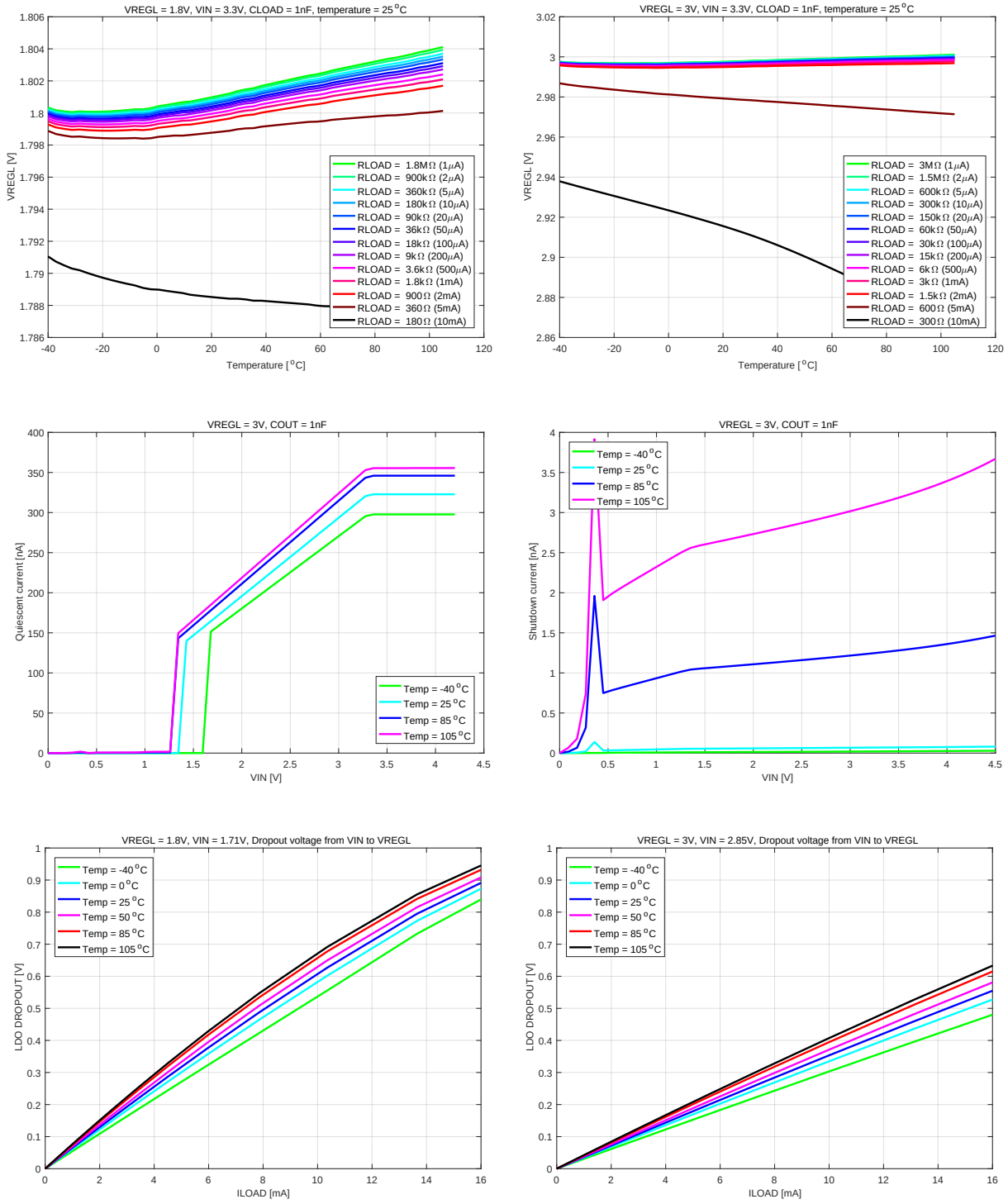


Figure 9: Typical characteristics of VREGL LDO regulator. (Part 4)

$T_J = 25°C$, $VDD = VREGL + 0.3V$, $I_{LOAD} = 10\mu A$ and $C_{LOAD} = 1nF$ unless otherwise noted.

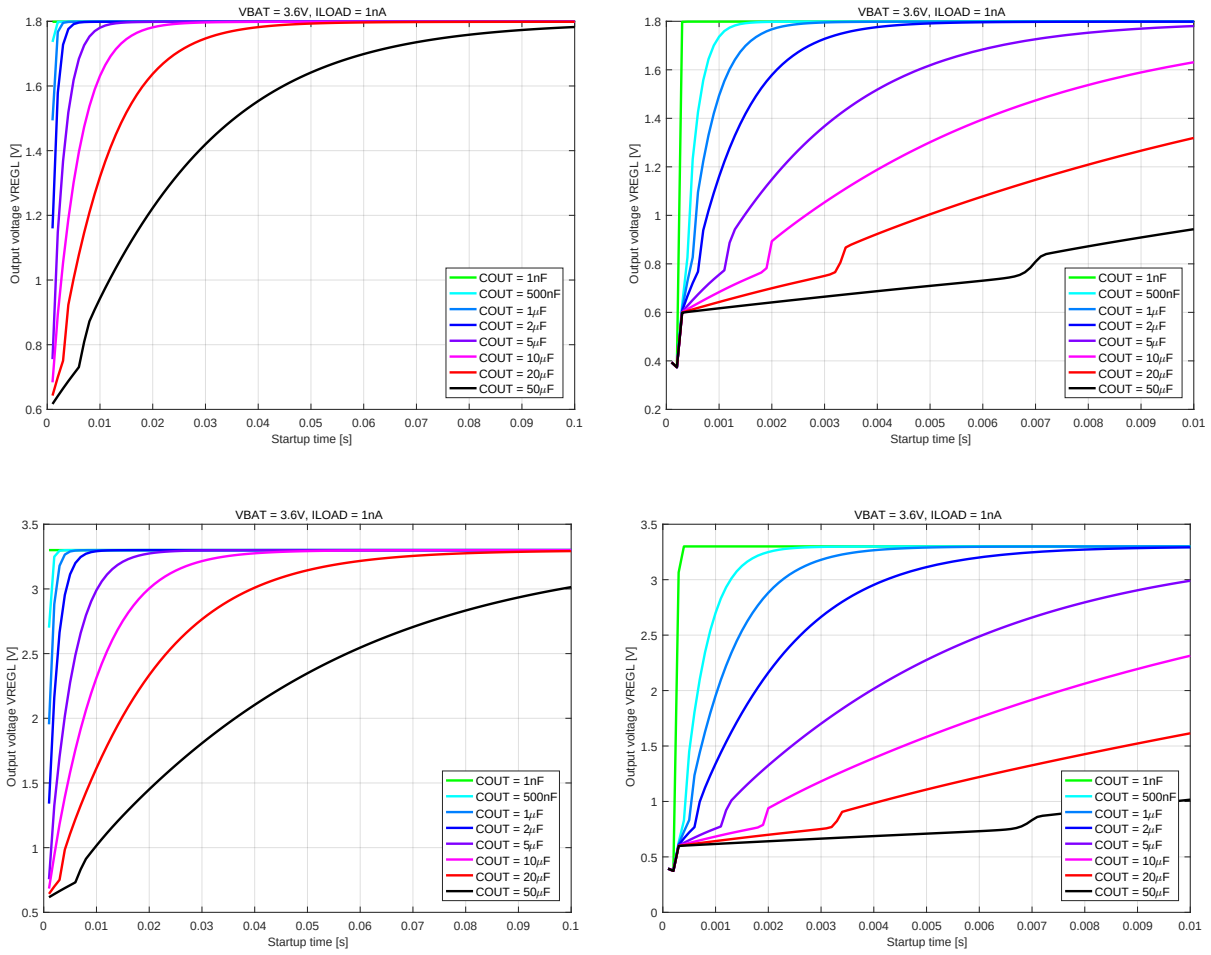


Figure 10: Typical characteristics of VREGL LDO regulator. (Part 5)

GLOAD: SWITCHED GROUND

ROCKY100 includes a dedicated pin to connect the ground of the load. This net is not directly connected to VSS but through an analog switch. This switch is kept open during the start-up of the device, so that no current drain is produced from the sensor.

This switch can be open and closed automatically commanded by VDD MONITOR or can be manually controlled by the user (refer to section PSM in page 41 for further details). Make sure the VDD monitor is configured correctly prior to connecting any load in automatic switching mode.

The following graphs show the detailed characteristics of the GLOAD switch.

Over the operating temperature range of T = -40 °C to 85 °C, VDD = 3V, unless otherwise noted.

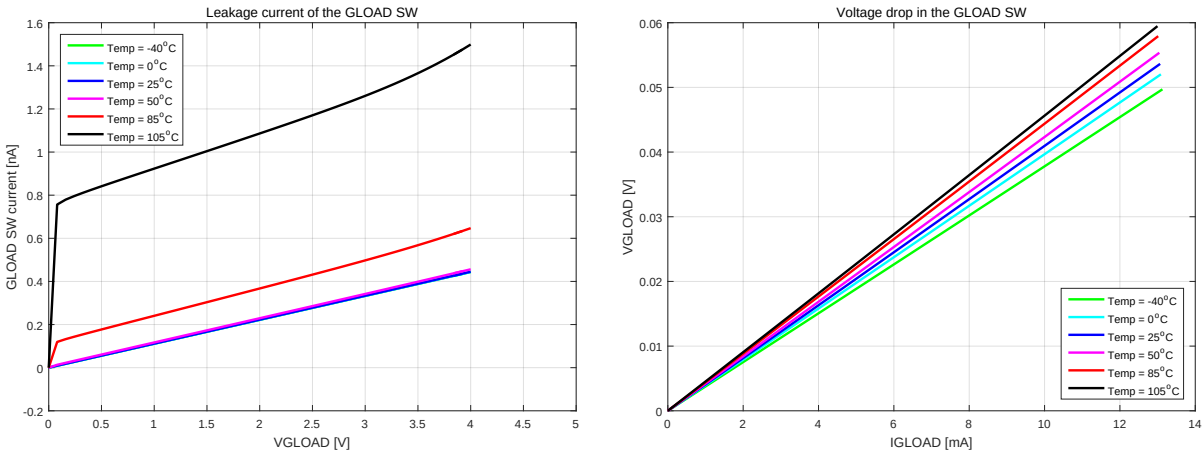


Figure 11: Detailed characteristics of GLOAD switch.

VDD MONITOR: LOAD SWITCHING

In order to avoid start-up oscillation, the load should be connected only after enough energy has been harvested to support its initialization. For this purpose, the VDD voltage is monitored and compared to two threshold values VLOADON and VLOADOFF. Once VDD is over VLOADON, the output of VREGL is enabled and the GLOAD switch is closed if automatic control is enabled.

If the VDD voltage drops below VLOADOFF, the output of VREGL is disabled and the GLOAD switched is open. This way, unexpected current rushes of the load in the out of specification regions are avoided.

Integrated trimming resistors are used to configure the feedback values of the VDD monitor. The threshold voltages VLOADON and VLOADOFF can be set modifying the TRIM_PSM register.

If the VDD monitor feature is not required in a specific application, it can be disabled in order to reduce the current consumption of the device.

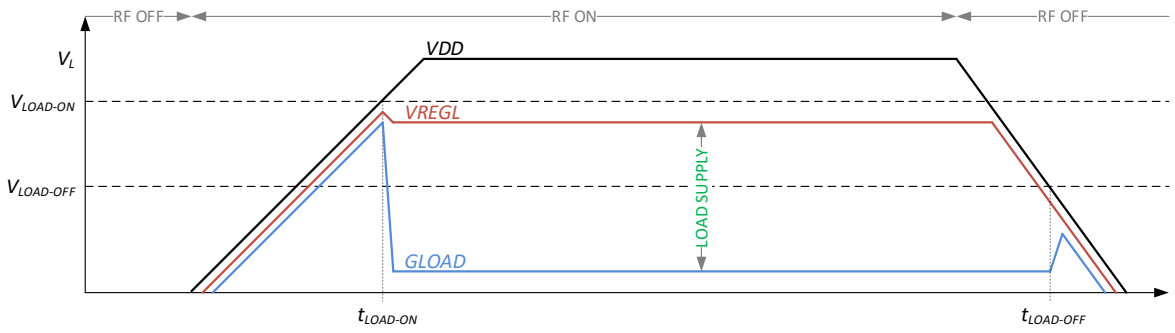


Figure 12: Functional diagram of VDD MONITOR and switched load supply.

MEMORY SPACE DEFINITION

The EPC Class-1 Generation-2 protocol defines a unique memory space divided in four banks: Reserved memory, EPC memory, TID memory and User memory. However, unlike traditional tags, this IC includes different physical devices which have to be addressed from the reader. Thus, a memory map table has been defined in order to be able to access any of the physical devices from the unique memory space defined in the communication standard.

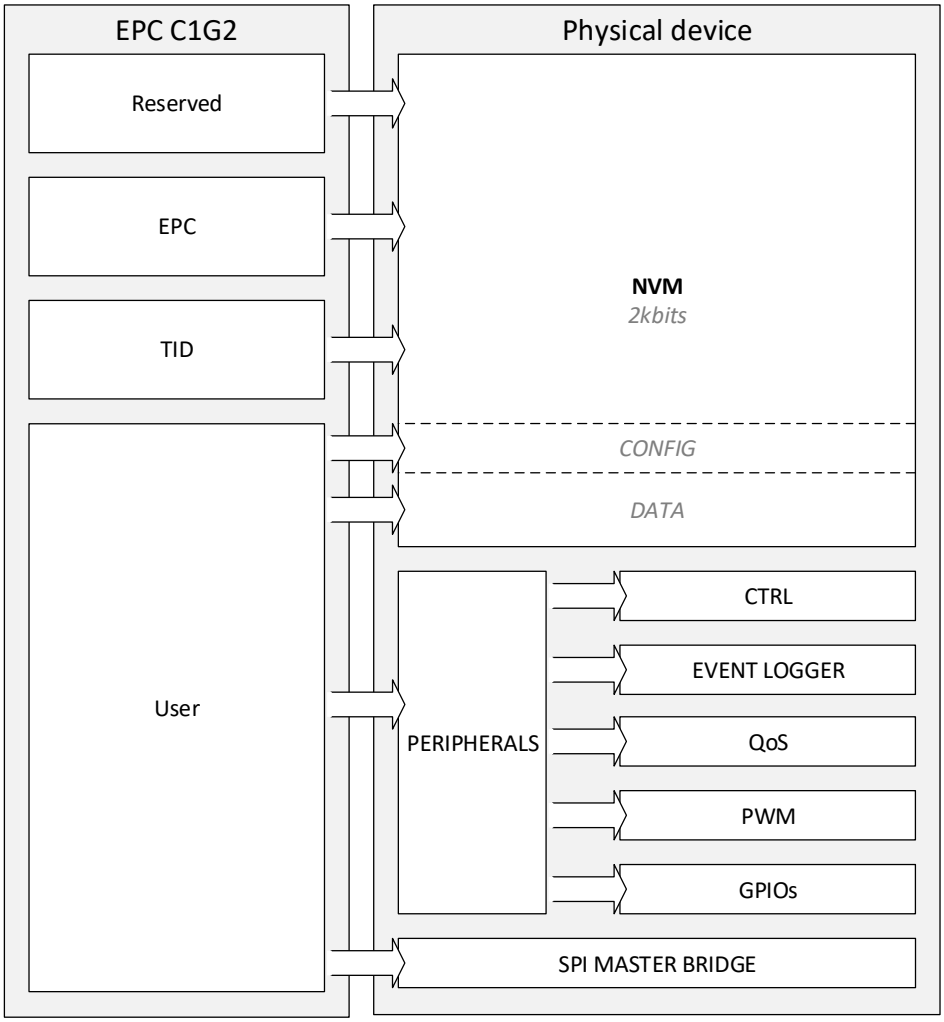


Figure 13: Memory space definition.

Figure 13 shows the generic structure used to map the EPC C1G2 memory space to the different devices included in the IC. As the Reserved, EPC and TID memory banks have to follow a standard-defined structure for its contents, the User memory bank is used to access the additional resources of the tag.

Some addresses of the User memory are mapped to the non volatile memory. The non volatile content from

the user memory is divided in two types of data: configuration and user data. The configuration portion of the non volatile memory is further divided into blocks of 16 consecutive registers ranging from addresses 0x00X0 to 0x00XF. ROCKY100 contains three of such configuration blocks, labeled from ConfBlock0 to ConfBlock2. Other addresses of the User memory are mapped to the internal peripherals of the IC: control, event logger, QoS, PWM and GPIOs. Some of those peripherals just provide information and their corresponding registers can only be read. Others are used to trigger actions, and can only be written. And the rest can be both read and written. Take care of making good use of each register in order to obtain the correct functionality.

Finally, the remaining addresses of the User memory are mapped to the SPI master bridge. The reason of mapping all remaining addresses to this device is that the received register address is used to send data through the MOSI pin.

The peripheral base address and the SPI master bridge base address are set to default values on manufacturing. But these values can be changed in order to prevent the loss of some functionality if the reader used to control the IC has limited addressing capabilities.

The memory map of the internal registers is shown in tables 1 to 4. The addressing of the registers consists on a memory bank identifier plus the physical address inside this memory bank.

A detailed description of each register can be found in the following sections.

Table 1: Memory map (part 1).

ADDRESS	REGISTER	DESCRIPTION
RESERVED *memory bank (non-volatile)*		
0x00	KILL_PWD_H	Kill password 16 MSB
0x01	KILL_PWD_L	Kill password 16 LSB
0x02	ACCESS_PWD_H	Access password 16 MSB
0x03	ACCESS_PWD_L	Access password 16 LSB
0x04	SILICON_REV	Tag hardware revision identifier
0x05	CURRENT_PBA	Peripheral Base Address being used by the IC
0x06	CURRENT_SBA	SPI Base Address being used by the IC
EPC *memory bank (non-volatile)*		
0x00	STORED_CRC	Stored CRC value
0x01	STORED_PC	Protocol-control word
0x02	EPC_0	Word 0 (MSB) of the EPC
0x03	EPC_1	Word 1 of the EPC
0x04	EPC_2	Word 2 of the EPC
0x05	EPC_3	Word 3 of the EPC
0x06	EPC_4	Word 4 of the EPC
0x07	EPC_5	Word 5 of the EPC
0x08	EPC_6	Word 6 of the EPC
0x09	EPC_7	Word 7 (LSB) of the EPC
TID *memory bank (non-volatile)*		
0x00	SHORT_TAG_ID_0	First word of the short tag identification
0x01	SHORT_TAG_ID_1	Second word of the short tag identification
0x02	XTID	Extended tag identification header
0x03	SN_SEG_0	Bits 47-32 of the Serial Number Segment
0x04	SN_SEG_1	Bits 31-16 of the Serial Number Segment
0x05	SN_SEG_2	Bits 15-0 of the Serial Number Segment

Table 2: Memory map (part 2).

ADDRESS	REGISTER	DESCRIPTION
***USER** memory bank - ConfBlock 0 (non-volatile)*		
0x00	OPMODE_CTL_NV	Operation mode non-volatile control word
0x01	TRIM_C1G2OSC	Trimming bits for C1G2 oscillator
0x02	PSM_CTL	Trimming bits for VLOAD domain (part 2)
0x03	TRIM_VLON	Trimming bits for VLOAD ON monitor
0x04	TRIM_VLOFF	Trimming bits for VLOAD OFF monitor
0x05	TRIM_VREGL	Trimming bits for VREGL feedback
0x06	GPIO0_CTL	GPIO0 control word
0x07	GPIO1_CTL	GPIO1 control word
0x08	GPIO2_CTL	GPIO2 control word
0x09	GPIO3_CTL	GPIO3 control word
0x0A	GPIO4_CTL	GPIO4 control word
0x0B	SPI_MASTER_CTL	SPI master control word
0x0C	QOS_CTL	QoS control word
0x0D	PER_BASE_ADDR	Peripheral partition base address
0x0E	SPI_BASE_ADDR	SPI partition base address
0x0F	CFG_LOCK_0	Configuration block word 0

Table 3: Memory map (part 3).

ADDRESS	REGISTER	DESCRIPTION
***USER** memory bank - ConfBlock1 (non-volatile)*		
0x10	CFG_READ_1	Peripheral configuration read block word 1
0x11	TRIM_ULFOSC	Trimming bits for ULF oscillator
0x12 ... 0x19	RFU	Reserved for future use
0x1A	WDT_CTL	Watchdog control word
0x1B	EDGE_CTL	Edge module control word
0x1C	SPI_OFFSET_H	Most significant bits of the SPI offset register
0x1D	SPI_OFFSET_L	Least significant bits of the SPI offset register
0x1E	LTC_CTL	Log Time Counter control word
0x1F	CFG_LOCK_1	Configuration block word 1

Table 4: Memory map (part 4).

ADDRESS	REGISTER	DESCRIPTION
***USER** memory bank - ConfBlock2 (non-volatile)*		
0x20	CFG_READ_2	Peripheral configuration read block word 2
0x21	LOG_CTL	Event logger module control word
0x22	LOG_NVCOUNT	Event logger non-volatile count
0x23	LOG_NVTSTAMP	Event logger non-volatile time-stamp
0x24	LOG_NVDATA	Event logger non-volatile data
0x25	PWM_CTL	PWM control word
0x26 ... 0x2E	RFU	Reserved for future use
0x2F	CFG_LOCK_2	Configuration block word 2
***USER** memory bank - User data (non-volatile)*		
0x30 ... 0x6E	USER_DATA	Free memory for user data (Up to 1.008 bits, depending on CURRENT_PBA)

Table 5: Memory map (part 5).

ADDRESS	REGISTER	DESCRIPTION
***USER** memory bank - Peripheral partition (volatile, referred to CURRENT_PBA)*		
0x00	REBOOT	Soft reboot trigger
0x01	OPMODE_CTL_V	Operation mode volatile control word
***USER** memory bank - Event logger peripheral (volatile, referred to CURRENT_PBA)*		
0x02	LTC	LTC counter
0x03	LOG_VCOUNT	Event logger volatile count
0x04	LOG_VTSTAMP	Event logger volatile time-stamp
0x05	LOG_VDATA	Event logger volatile data
***USER** memory bank - Quality of Service peripheral (volatile, referred to CURRENT_PBA)*		
0x0F	QOS_BITS	Currently read QoS value of the tag
0x10	RESERVED	Unspecified tag information
***USER** memory bank - PWM peripheral (volatile, referred to CURRENT_PBA)*		
0x11	PWM_TRIGGER	PWM trigger
***USER** memory bank - GPIO read/write peripheral (volatile, referred to CURRENT_PBA)*		
0x12	GPIO_READ	Values read from the input GPIO pins
0x13	GPIO_WRITE	Values to write to the output GPIO pins
***USER** memory bank - SPI master module (volatile, referred to CURRENT_SBA)*		
0x00 ...	SPI MASTER	Bridge to SPI master module

EPC C1G2

RESERVED MEMORY BANK

KILL_PWD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KILL_PWD_H															

Memory bank: Reserved
Address: 0x00
Type: R/W
Factory value: 0x0000
Description: Kill password 16 MSB.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KILL_PWD_L															

Memory bank: Reserved
Address: 0x01
Type: R/W
Factory value: 0x0000
Description: Kill password 16 LSB.

The KILL_PWD_H and KILL_PWD_L words compose the *Kill password* of the EPC Class-1 Generation-2 tag. The MSB of the password are stored in KILL_PWD_H, whereas the LSB are stored in KILL_PWD_L.

ACCESS_PWD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESS_PWD_H															

Memory bank: Reserved
Address: 0x02
Type: R/W
Factory value: 0x0000
Description: Access password 16 MSB.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACCESS_PWD_L															

Memory bank: Reserved

Address: 0x03

Type: R/W

Factory value: 0x0000

Description: Access password 16 LSB.

The ACCESS_PWD_H and ACCESS_PWD_L words compose the *Access password* of the EPC Class-1 Generation-2 tag. The MSB of the password are stored in ACCESS_PWD_H, whereas the LSB are stored in ACCESS_PWD_L.

SILICON_REV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SILICON_REV															

Memory bank: Reserved

Address: 0x04

Type: R

Factory value: 0xFA3X

Description: Tag hardware revision identifier.

Silicon revision identifier of the IC.

CURRENT_PBA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_PBA															

Memory bank: Reserved

Address: 0x05

Type: R

Factory value: 0x0080

Description: Read-only Peripheral Base Address that is being used by the tag.

This register defines the base address of the peripheral address space. It is preloaded to the default value defined in PER_BASE_ADDR.

CURRENT_SBA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CURRENT_SBA															

Memory bank:	Reserved
Address:	0x06
Type:	R
Factory value:	0x0100
Description:	Read-only SPI Base Address that is being used by the tag.

This register defines the base address of the SPI address space. It is preloaded to the default value defined in SPI_BASE_ADDR.

EPC MEMORY BANK

STORED_CRC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STORED_CRC															

Memory bank: EPC

Address: 0x00

Type: R

Factory value: N/A

Description: CRC16 value of contents of PC+EPC.

Every time the tag is powered up, it operates the CRC16 value of the content of PC+EPC bits. This value is stored in internal volatile registers, and is readable through this register. The STORED_CRC value is recalculated every time the tag is powered up or soft-rebooted and cannot be overwritten.

STORED_PC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_length					**UMI**	**XI**	**NSI**								

Memory bank: EPC

Address: 0x01

Type: R/W

Factory value: 0x3100

Description: Protocol-control word.

[15-11] **EPC_length:** The length of the EPC, in words.

[10] **UMI:** User memory indicator.

- **'0'**: User memory contains no information
- **'1'**: User memory contains information

[9] **XI:** XPC_W1 indicator.

- **'0'**: XPC_W1 is not used
- **'1'**: XPC_W1 is used

[8-0] **NSI:** Numbering system identifier.

If the value written into EPC_length is not supported by ROCKY100 (it is null or greater than 8), then ROCKY100 will operate as if STORED_PC was programmed with a value of 0x3500.

EPC

The EPC_0, EPC_1, EPC_2, EPC_3, EPC_4, EPC_5, EPC_6 and EPC_7 words compose the *Electronic Product Code* (EPC) of the EPC Class-1 Generation-2 tag. The MSB of the EPC are stored in EPC_0, whereas the LSB are stored in EPC_7.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_0															

Memory bank: EPC
Address: 0x02
Type: R/W
Factory value: Unique EPC value.
Description: Word 0 (MSB) of the EPC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_1															

Memory bank: EPC
Address: 0x03
Type: R/W
Factory value: Unique EPC value.
Description: Word 1 of the EPC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_2															

Memory bank: EPC
Address: 0x04
Type: R/W
Factory value: Unique EPC value.
Description: Word 2 of the EPC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_3															

Memory bank: EPC
Address: 0x05
Type: R/W
Factory value: Unique EPC value.
Description: Word 3 of the EPC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_4															

Memory bank: EPC

Address: 0x06

Type: R/W

Factory value: Unique EPC value.

Description: Word 4 of the EPC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_5															

Memory bank: EPC

Address: 0x07

Type: R/W

Factory value: Unique EPC value.

Description: Word 5 of the EPC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_6															

Memory bank: EPC

Address: 0x08

Type: R/W

Factory value: Unique EPC value.

Description: Word 6 of the EPC.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EPC_7															

Memory bank: EPC

Address: 0x09

Type: R/W

Factory value: Unique EPC value.

Description: Word 7 (LSB) of the EPC.

TID MEMORY BANK

SHORT_TAG_TID (CONSTANT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHORT_TAG_TID_0															

Memory bank: TID

Address: 0x00

Type: R

Factory value: 0xE282

Description: First word of the short tag identification register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHORT_TAG_TID_1															

Memory bank: TID

Address: 0x01

Type: R

Factory value: 0x8001

Description: Second word the the short tag identification register.

XTID (CONSTANT)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
XTID															

Memory bank: TID

Address: 0x02

Type: R

Factory value: 0x2000

Description: Extended Tag Identification.

SN_SEG

The SN_SEG_0, SN_SEG_1 and SN_SEG_2 words compose the *Serial number segment* of the TID memory bank. The MSB of the serial number segment are stored in SN_SEG_0, whereas the LSB are stored in SN_SEG_2.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN_SEG_0															

Memory bank: TID

Address: 0x03

Type: R/W

Factory value: Unique TID value

Description: First (MS) word of the serial number segment of the TID memory bank.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN_SEG_1															

Memory bank: TID

Address: 0x04

Type: R/W

Factory value: Unique TID value

Description: Second word of the serial number segment of the TID memory bank.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SN_SEG_2															

Memory bank: TID

Address: 0x05

Type: R/W

Factory value: Unique TID value

Description: Last (LS) word of the serial number segment of the TID memory bank.

USER MEMORY BANK

The User memory bank of ROCKY100 is mapped to configuration data, user data and peripheral control. The following sections provide a detailed description of the configuration and control registers related to each peripheral.

The user data section can be freely used to store the application data desired by the end user.

PERIPHERAL BASE ADDRESS

The base address of the peripheral partition of ROCKY100 is user programable through register PER_BASE_ADDR. This means that the mapping of all peripherals described in table 5 is controlled with this register. Although any value can be stored in PER_BASE_ADDR, the following restrictions apply to ROCKY100 :

- The peripheral base address corresponds with the 14 least significant bits of register PER_BASE_ADDR.
- The peripheral base address must not fall within the range of the configuration partition of ROCKY100 (memory addresses from 0x00 to 0x2F of the user memory bank).

If the peripheral base address obtained from PER_BASE_ADDR is invalid, ROCKY100 will assume a default peripheral base address of 0x0030. Bear in mind that in this circumstance no user data memory will be available to the user.

The actual peripheral base address being use by ROCKY100 can be read from register CURRENT_PBA at address 0x05 of the reserved memory bank.

PERIPHERAL BASE ADDRESS REGISTER

PERIPHERAL_BASE_ADDRESS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU		**PERIPHERAL_BASE_ADDR**													

Memory bank: User

Address: 0x0D

Type: R/W

Factory value: 0x0080

Description: Peripheral base address register.

[13 - 0] **PERIPHERAL_BASE_ADDR**.

SPI BASE ADDRESS

The first user memory bank address that is mapped to the SPI Master bridge in ROCKY100 is user configurable through register SPI_BASE_ADDR. Although any value can be stored in SPI_BASE_ADDR, the following restrictions apply to ROCKY100 :

- The SPI base address corresponds with the 15 least significant bits of register SPI_BASE_ADDR.
- The SPI base address must be at greater than the peripheral base address being used by ROCKY100 (CURRENT_PBA). This guarantees that the reboot peripheral is always accessible.

If the SPI base address obtained from SPI_BASE_ADDR is illegal, ROCKY100 will assume a default SPI base address equal to CURRENT_PBA plus one. Bear in mind that in this circumstance only the reboot peripheral will be accessible in the memory space of ROCKY100 .

The actual SPI base address being use by ROCKY100 can be read from register CURRENT_SBA at address 0x06 of the reserved memory bank.

SPI BASE ADDRESS REGISTER

SPI_BASE_ADDRESS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU	**SPI_BASE_ADDR**														

Memory bank: User

Address: 0x0E

Type: R/W

Factory value: 0x0100

Description: SPI base address register.

[14 - 0] **SPI_BASE_ADDR**.

OPERATION MODE

ROCKY100 can be configured to operate in different operation modes. Some of those configurations are intended for test purposes, whereas others can be configured to optimize the efficiency of the device for a specific application. Setting these configurations incorrectly can cause the device to stop working. Moreover, it can be interesting for some applications to change some of those configuration only for a single run, so that the original configuration is recovered after resetting the device.

In order to offer all these options, the operation mode configurations can be set by two means: volatile configuration and non-volatile configuration. If the volatile configuration is changed, once the power source is removed the configuration is lost. If the non-volatile configuration is changed, even after a power source cut the configuration will be kept.

The default configuration of ROCKY100 is specified in the non-volatile operation mode control register. If a write operation modifies the contents of the volatile operation mode register, then ROCKY100 will be configured in accordance to this value. In this case, the configuration stored in the non-volatile operation mode control register will be ignored until ROCKY100 is powered down.

Register	User memory address	Operation mode control register
OPMODE_CTL_NV	0x00	Non-volatile control register
OPMODE_CTL_V	CUR_PBA + 0x01	Volatile control register

ASK MODE

ROCKY100 includes two different ASK demodulators for the forward link: the passive demodulator and the high sensitivity demodulator. The high sensitivity demodulator has a higher power consumption than the passive demodulator. Thus, it is intended to be used in BAP applications. Moreover, the high sensitivity demodulator has a lower saturation input power. In order to cover the complete RF input power range, ROCKY100 has to switch between both demodulators. The behavior of this switching can be configured through the ASKSEL parameter.

ASKSEL	ASK demodulator selector
’000’	Passive demodulator
’001’	High sensitivty demodulator
’011’	Automatic selection

The ASK demodulator selector is overrided if any of the GPIOs of ROCKY100 is configured in ASK bypass mode (refer to section GPIO CONFIGURATION in page 44 for further details). If several GPIOs are simultaneously configured in ASK bypass mode, then the GPIO with the highest identifier (GPIO4 in case all GPIOs are configured in this mode) will override the ASK demodulator selector value.

ROCKY100 also allows inverting the output of the selected ASK signal (ASKSEL or GPIO bypass). The ASKPOL parameter allows configuring this feature. In order to use the integrted C1G2 processor, ASKPOL has to be set to ’0’.

ASKPOL	ASK polarity selector
’0’	ASK follows envelope of RF signal
’1’	ASK is inverse to envelope of RF signal

BAP MODE

ROCKY100 is prepared to be used both in passive and BAP applications. For the latter ones, a dedicated VBAT pin is included. This pin can be connected to VDD by means of an integrated battery switch. This switch is intended to minimize battery drain of BAP tags prior to activation. The switch can be controlled through the BATSW parameter.

BATSW	Battery switch control
'0'	Switch open. Battery supply not connected to VDD
'1'	Switch closed. Battery supply connected to VDD

Moreover, the high sensitivity demodulator may be activated in order to extend the communication range of the device. In such a configuration, a higher current consumption shall be expected. The following configurations are available.

BAPSENS	Sensitivity	Increment in I_{DD}
'000'	-24dBm	-
'111'	-35dBm	2 μA

Note that BAPSENS only enables the high sensitivity demodulator. In order to achieve the highest sensitivity values, the ASKSEL parameter should correctly point to the high sensitivity demodulator.

PSK MODE

The modulation depth of the backscattered signal depends on the PSK modulator. The deeper the modulation is, the higher the SNR of the backward communication link will be under same circumstances. However, the deeper the modulation is, the lower the harvested energy during backscattering will be. Thus, depending on the application, it may be more interesting to increase or decrease the modulation depth.

ROCKY100 allows configuring the modulation depth through the PSKSEL parameter. PSKSEL is a 4 bit parameter. Each bit of PSKSEL can be independently configured. Enabling only the least significant bit of PSKSEL produces the lowest PSK modulation supported by ROCKY100, but maximizes the harvested energy.

PSKSEL	PSK modulation depth selector
'0000'	No modulation
'0001'	Lowest modulation
...	...
'1000'	Medium modulation
...	...
'1111'	Highest modulation

RNG MODE

The C1G2 core processor requires a Random Number Generator (RNG) for the anti-collision algorithm and data masking. ROCKY100 can be configured to use either a true random number generator or a pseudo random generator. The pseudo random generator requires a seed as starting point. This seed is defined as the value in the TRIM_C1G2OSC register.

RNG	Random Number Generation mode
’0’	Pseudo-random
’1’	True random

C1G2 OSCILLATOR

C1G2 oscillator trimming bits. Sets the internal operation frequency of the digital processor. This value shall be configured so that generated frequency is close to 1.92MHz.

ULF OSCILLATOR

Ultra Low Frequency (ULF) oscillator trimming bits. Sets the internal operation frequency of the Log Time Counter (LTC) time base generator. This value shall be configured so that the generated frequency is close to 1Hz.

OPERATION MODE REGISTERS

OPMODE_CTL_NV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU		RST_SESSION	RNG	PSKSEL				ASKSEL			ASKPOL	BATSW	BAPSENS		

Memory bank: User

Address: 0x00

Type: R/W

Factory value: 0x1F00

Description: Operation mode volatile control word.

[13] **RST_SESSION:** ASK watchdog events reset S0, S2, S3 and SL flags

- **'0'**: reset disabled.
- **'1'**: reset enabled.

[12] **RNG:** random number generator mode.

- **'0'**: pseudo-random mode.
- **'1'**: true random mode.

[11:8] **PSKSEL:** PSK modulation depth selector.

[7:5] **ASKSEL:** ASK source selector.

- **'000'**: Passive demodulator.
- **'001'**: High sensitivity demodulator.
- **'011'**: Automatic selection.

[4] **ASKPOL:** ASK polarity selector.

- **'0'**: ASK follows envelope of RF signal.
- **'1'**: ASK is inverse to envelope of RF signal.

[3] **BATSW:** Battery switch control.

- **'0'**: switch open. Battery supply not connected to VDD.
- **'1'**: switch closed. Battery supply connected to VDD.

[2:0] **BAPSENS:** communications sensitivity configuration in BAP mode.

- **'000'**: -24dBm.
- **'111'**: -30dBm.

OPMODE_CTL_V

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU		RST_SESSION	RNG	PSKSEL				ASKSEL			ASKPOL	BATSW	BAPSENS		

Memory bank: User

Address: CUR_PBA + 0x01 (Default: 0x81)

Type: W

Factory value: 0x00

Description: Operation mode volatile control word.

[13] **RST_SESSION:** ASK watchdog events reset S0, S2, S3 and SL flags

- **'0'**: reset disabled.
- **'1'**: reset enabled.

[12] **RNG:** random number generator mode.

- **'0'**: pseudo-random mode.
- **'1'**: true random mode.

[11:8] **PSKSEL:** PSK modulation depth selector.

[7:5] **ASKSEL:** ASK source selector.

- **'000'**: Passive demodulator.
- **'001'**: High sensitivity demodulator.
- **'011'**: Automatic selection.

[4] **ASKPOL:** ASK polarity selector.

- **'0'**: ASK follows envelope of RF signal.
- **'1'**: ASK is inverse to envelope of RF signal.

[3] **BATSW:** Battery switch control.

- **'0'**: switch open. Battery supply not connected to VDD.
- **'1'**: switch closed. Battery supply connected to VDD.

[2:0] **BAPSENS:** communications sensitivity configuration in BAP mode.

- **'000'**: -24dBm.
- **'111'**: -30dBm.

TRIM_C1G2OSC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIM_C1G2OSC															

Memory bank: User

Address: 0x01

Type: R/W

Factory value: 0x00

Description: Trimming value for C1G2 oscillator.

C1G2 oscillator trimming bits. Sets the internal operation frequency of the digital processor. This value shall be configured so that generated frequency is close to 1.92MHz.

TRIM_ULFOSC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIM_ULFOSC															

Memory bank: User

Address: 0x11

Type: R/W

Factory value: 0x00

Description: Trimming value for ULF oscillator.

PSM CONTROL

The threshold voltages VLOADON, VLOADOFF and the output voltage of VREGL can be set following the next equations:

$$CODE_{dec} = 1183 - 256\left(\frac{V}{0.6} - 1\right) \tag{1}$$

The following table shows three examples of possible VLOAD configuration:

Table 6: VLOAD configuration examples.

	Example 1		**Example 2**		**Example 3**	
	V	**code**	**V**	**code**	**V**	**code**
VREGL	1.5	0x31F	2	0x249	3	0x09F
VLOADON	1.7	0x2CA	2.2	0x1F4	3.1	0x074
VLOADOFF	1.4	0x34A	1.9	0x274	2.9	0x0CA

Additionally, the output of the voltage monitors used to control startup of the tag and the load can be accessed for Quality of Service purposes. The SPI master module adds this information when triggered. Nevertheless, it is also possible to read the current state of this signals through the QOS_BITS register.

PSM CONTROL REGISTERS

PSM_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU									RFU_0		VREGL_MODE		GLOAD_MODE		VLMON_EN

Memory bank: User

Address: 0x02

Type: R/W

Factory value: 0x0000

Description: PSM control word.

[6:5] **RFU_0:** Control word reserved for future use. It must be set to all zeros.

[4:3] **VREGL_MODE:** VREGL switch mode.

- **'00'**: Off.
- **'10'**: Auto.
- **'01'**: On.

[2:1] **GLOAD_MODE:** GLOAD switch mode.

- **'00'**: Off.
- **'10'**: Auto.
- **'01'**: On.
- **'11'**: PWM output.

[0] **VLMON_EN:** VLOAD monitor enable.

- **'0'**: Disabled.
- **'1'**: Enabled.

TRIM_VLON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU						TRIM_VLON									

Memory bank: User

Address: 0x03

Type: R/W

Factory value: 0x0174 (2.5V)

Description: VLON trimming word.

[9:0] **TRIM_VLON:** VLOAD ON threshold voltage. Refer to equation 1.

TRIM_VLOFF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU						TRIM_VLOFF									

Memory bank: User

Address: 0x04

Type: R/W

Factory value: 0x029F (1.8V)

Description: VLOFF trimming word.

[9:0] **TRIM_VLOFF:** VLOAD OFF threshold voltage. Refer to equation 1.

TRIM_VREGL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU						TRIM_VREGL									

Memory bank: User

Address: 0x05

Type: R/W

Factory value: 0x0249 (2.0V)

Description: VREGL trimming word.

[9:0] **TRIM_VREGL:** VREGL output voltage. Refer to equation 1.

QOS_BITS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU												Q3	Q2	Q1	Q0

Memory bank: User

Address: CUR_PBA + 0x0F (Default: 0x8F)

Type: R

Factory value: 0x00

Description: Quality of Service register.

[3] **Q3**: VDD is above VLOADON threshold (configured with TRIM_VLON) .

[2] **Q2:** VDD is above VLOADOFF threshold (configured with TRIM_VLOFF).

[1] **Q1:** VDD is above VTAGON threshold (1.2V).

[0] **Q0:** VDD is above VTAGOFF threshold (0.9V).

GPIO

ROCKY100 includes 5 General Purpose Input Output pins. Each of them can be individually configured to select the desired function. Weak pull (up or down) resistors can be configured in case they are needed.

Additionally, the functionality of the pin has to be mapped to the SPI master, SPI slave, event generator or signal bypass module. For SPI modules, the behavior of each pin is predefined. For events and bypass signals, further configuration is required to select the specific signal. Tables 7 to 10 show the available options.

In case GPIO_IN is used, then the GPIO is configured as an input and its logical value can be read through register GPIO_READ. In case GPIO_OUT is used, then the GPIO is configured as an output and its logical value is set by writing to the GPIO_WRITE register.

Table 7: SIGSEL definition when **DEVSEL = '10'** (event generator).

SIGSEL	Event	Description
0x00	command_start	The tag has started processing a new C1G2 command
0x01	command_stop	The tag has stopped processing a C1G2 command
0x02	select_matched	A valid select command has been received that has asserted the matched flag
0x03	select_mask_matched	A valid select command with no null mask has been received that has asserted the matched flag
0x04	select_unmatched	A valid select command has been received that has deasserted the matched flag
0x05	select_mask_unmatched	A valid select command has been with no null mask has been received that has deasserted the matched flag
0x07	null_slot_counter	The slot counter has a null value after processing a Query, QueryAdjust or QueryRep command
0x08	access_UM_NVM	A memory access to the UM located in NVM has been processed
0x09	access_UM_config	A memory access targeted to the configuration registers of the UM bank has been processed
0x0B	access_SPI_master	A memory access targeted to the SPI bridge has been processed
0x0C	symbol_timeout	The watchdog in SYMBOL has timed out
0x0D	reboot_or_por	PoR condition or the control unit of R100 has been rebooted
0x0E	reboot	The control unit of R100 has been rebooted

Table 8: SIGSEL definition when **DEVSEL = '11'** (signal bypass).

SIGSEL	Signal	Direction	Description
0x00	GPIO_IN	Input	The value read on the pin is copied into GPIO_READ
0x01	GPIO_OUT	Output	The value of GPIO_WRITE is copied in the output buffer of the pad
0x02	PWM	Output	Output of the PWM generator
0x03	EDGE_1_IN	Input	Input source to the first edge detector peripheral. If several GPIOs are configured simultaneously in this mode, then the GPIO with the highest identifier (GPIO4, GPIO3, ...) has preference
0x04	EDGE_2_IN	Input	Input source to the second edge detector peripheral. If several GPIOs are configured simultaneously in this mode, then the GPIO with the highest identifier (GPIO4, GPIO3, ...) has preference
0x05	EDGE_1_OUT	Output	Outputs the event of the first edge detector peripheral
0x06	EDGE_2_OUT	Output	Outputs the event of the second edge detector peripheral
0x07	EVENLOG_MTP	Output	On high indicates that the event logger is accessing the MTP memory
0x08	SPI_MODE	Input	When GPIO4 is configured in this mode, the logical value read from the pad will force an SPI mode on the remaining GPIOs. When GPIO4 = '0', the remaining GPIOs will be configured in SPI master mode. When GPIO4 = '1', the remaining GPIOs will be configured in SPI slave mode
0x09	SPI_MASTER_CS	Output	Outputs the CS signal of the SPI master bridge
0x0A	SPI_MASTER_SCK	Output	Outputs the SCK signal of the SPI master bridge
0x0B	SPI_MASTER_MOSI	Output	Outputs the MOSI signal of the SPI master bridge
0x0C	SPI_MASTER_MISO	Input	Connects the value read from the GPIO to the MISO port of the SPI master bridge. If several GPIOs are configured simultaneously in this mode, the GPIO with the highest identifier takes preference. GPIO0 in SPI master mode has preference over this configuration
0x0D	SPI_SLAVE_CS	Input	Connects the value read from the GPIO to the CS port of the SPI slave bridge. If several GPIOs are configured simultaneously in this mode, the GPIO with the highest identifier takes preference. GPIO3 in SPI slave mode has preference over this configuration
0x0E	SPI_SLAVE_SCK	Input	Connects the value read from the GPIO to the SCK port of the SPI slave bridge. If several GPIOs are configured simultaneously in this mode, the GPIO with the highest identifier takes preference. GPIO2 in SPI slave mode has preference over this configuration

Table 9: SIGSEL definition when **DEVSEL = '11'** (signal bypass) (continued).

SIGSEL	Signal	Direction	Description
0x0F	SPI_SLAVE_MOSI	Input	Connects the value read from the GPIO to the MOSI port of the SPI slave bridge. If several GPIOs are configured simultaneously in this mode, the GPIO with the highest identifier takes preference. GPIO1 in SPI slave mode has preference over this configuration
0x10	SPI_SLAVE_MISO	Output	Outputs the MISO signal of the SPI slaveter bridge
0x11	VLOAD_OK	Output	On high indicates that the regulated output meets the PSM configuration
0x12	QoS_7	Output	Not implemented
0x13	QoS_6	Output	Not implemented
0x14	QoS_5	Output	Not implemented
0x15	QoS_4	Output	Not implemented
0x16	QoS_3	Output	VTAG is above VTAGOFF threshold (0.8V)
0x17	QoS_2	Output	VTAG is above VTAGON threshold (1.4V)
0x18	QoS_1	Output	VLOAD is above VLOADOFF threshold (configured with TRIM_VLOFF)
0x19	QoS_0	Output	VLOAD is above VLOADON threshold (configured with TRIM_VLON)
0x1A	PSK_internal	Output	PSK signal generated by the digital core
0x1B	PSK_external	Input	PSK signal provided by an external source. When this mode is enabled, the digital core is forced to an idle state and the tag behaves as an analog front end
0x1C	ASK	Output	ASK signal received from the analog front end
0x1D	HSASK	Output	HSASK signal received from the analog front end
0x1E	ASK_NO_PSK	Output	ASK signal received from the analog front end with backscattered PSK filtered
0x1F	ASK_EXT	Input	ASK signal provided by an external source. When this mode is enabled, the ASK configuration in OPMODE_CTL_NV and OPMODE_CTL_V is overridden and the digital core is loaded with ASK_EXT. If several GPIOs are configured simultaneously in ASK_EXT signal bypass mode, then the GPIO with the highest identifier (GPIO4, GPIO3, . . .) is selected

Table 10: SIGSEL definition when **DEVSEL = '11'** (signal bypass) (continued).

SIGSEL	Signal	Direction	Description
0x20	C1G2_OSC	Output	Clock signal of the C1G2 processor
0x21	LF_OSC	Output	Low Frequency clock signal
0x22	ULF_OSC	Output	ULF clock signal
0x23	RNG_ENABLE	Input	Forces the enable condition on the RNG oscillator
0x24	RNG_START	Input	Forces the start condition on the RNG oscillator
0x25	CLK_RNG	Output	Random number generator clock signal
0x2C	S1_FLAG	Output	On high indicates that session S1 is set to *B*

GPIO REGISTERS

GPIOx_CTL

15	14	13 12	11 10 9 8 7 6 5 4	3	2 1 0
REN	**RTIE**	**DEVSEL**	**SIGSEL**	**EVACTIVE**	**RFU**

Memory bank: User

Address: GPIO0: 0x06 | GPIO1: 0x07 | GPIO2: 0x08 | GPIO3: 0x09 | GPIO4: 0x0A

Type: R/W

Factory value: 0x3008.

Description: GPIOx control word.

[15] **REN:** pull resistor enable.

- **'0'**: pull resistor disabled.
- **'1'**: pull resistor enabled.

[14] **RTIE:** pull resistor tie configuration.

- **'0'**: pull resistor tied low.
- **'1'**: pull resistor tied high.

[13-12] **DEVSEL:** device to connect to the GPIO.

- **'00'**: master SPI.
- **'10'**: event generator.
- **'01'**: slave SPI.
- **'11'**: signal bypass.

[11-4] **SIGSEL:** signal source selector. Its meaning depends on the value of DEVSEL field:

- **DEVSEL = '10'**, refer to table 7.
- **DEVSEL = '11'**, refer to 8, 9 and 10.
- Ignored otherwise.

[3] **EVACTIVE:** active state of events.

- **'0'**: logic low.
- **'1'**: logic high.

GPIO_READ

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU											GPIO_READ				

Memory bank: User

Address: CURRENT_PBA + 0x12 (Default: 0x92)

Type: R

Factory value: 0x00

Description: Current value of GPIO_IN bypass signals.

This register reads out the current value in the GPIOs configured as GPIO_IN signal bypass. The logical value of GPIOx is read in bit position *x* of GPIO_READ.

Note that if the GPIOx_CTL control word of GPIOx is not configured such as DEVSEL = '11' (signal bypass) and SIGSEL = 0x00 (GPIO_IN), then bit position *x* in GPIO_READ contains meaningless data.

GPIO_WRITE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU											GPIO_WRITE				

Memory bank: User

Address: CURRENT_PBA + 0x13 (Default: 0x93)

Type: R/W

Factory value: 0x00

Description: Current value of GPIO_OUT bypass signals.

This register sets the current value in the GPIOs configured as GPIO_OUT signal bypass. The output logical value of GPIOx corresponds with the logical value of bit *x* of GPIO_WRITE.

Note that if the GPIOx_CTL control word of GPIOx is not configured such as DEVSEL = '11' (signal bypass) and SIGSEL = 0x01 (GPIO_OUT), then the logical value at bit position *x* in GPIO_WRITE will not be copied into the output buffer of the GPIOx pad.

SPI MASTER

ROCKY100 includes dedicated hardware for master SPI operation. The serial interface interacts with SPI slaves with 4 wires: CS, SCK, MOSI and MISO.

- **CS**: Chip Select signal to enable the slave device, driven by the SPI master.
- **SCK**: Serial Clock, driven by the SPI master.
- **MOSI**: Master Output Slave Input data port, driven by the SPI master.
- **MISO**: Master Input Slave Output data port, driven by the SPI slave.

SPI MASTER CONFIGURATION

ROCKY100 includes a flexible SPI master module. The behavior of the SPI master can be configured writing the desired configuration on the SPI_MASTER_CFG register. The following parameters can be configured:

IDLE state

The idle state of the I/O pads can be defined to be logic high or logic low. During normal operation of the tag, and while no SPI operation is being performed, all SPI related I/O pads will be kept in this state.

In order to define the desired idle state, set IDLE flag of SPI_CFG register as follows:

- **IDLE = 0**: The idle state of the I/O pads is logic low (≈VSS).
- **IDLE = 1**: The idle state of the I/O pads is logic high (≈VIO).

Given that the CS signal is commonly used to activate the SPI slave, the IDLE state has to be selected accordingly to the SPI slave connected to the device.

SPI mode

Even though the SPI communication is a common standard, it only defines the physical signaling between master and slave. Depending on when the data is read from the data lines and when written with respect to the clock signal, different SPI modes are defined.

Usually, the modes are determined by two parameters: the clock polarity and clock phase. ROCKY100 allows configuring the desired polarity and phase through the CPOL and CPHA bits in the SPI_CTL register.

Polarity:

- **CPOL = 0**: The initial state of the SCK line is logic low.
- **CPOL = 1**: The initial state of the SCK line is logic high.

Phase:

- **CPHA = 0**: Data is read from MISO and MOSI lines with the odd transitions of the SCK signal. Data is written to MISO and MOSI lines with the even transitions of the SCK signal. This means that the content of the first bit should be already pushed to the data lines before any transition of the SCK signal.
- **CPHA = 1**: Data is written from MISO and MOSI lines with the odd transitions of the SCK signal. Data is read to MISO and MOSI lines with the even transitions of the SCK signal.

SPI timing

The base clock frequency of the integrated SPI module is 1MHz. However, some devices may require lower frequencies to operate correctly. In order to slow down the SCK clock frequency, the DIVSCK parameter has to be configured in the SPI_CTL register.

- **DIVSCK = '00'**: /1 (f_{SCK} = 1MHz).
- **DIVSCK = '01'**: /2 (f_{SCK} = 500kHz).
- **DIVSCK = '10'**: /4 (f_{SCK} = 250kHz).
- **DIVSCK = '11'**: /8 (f_{SCK} = 125kHz).

Moreover, some SPI devices may require additional delays between I/O configuration, slave activation (CS) and data transmission (SCK). For this purpose, the parameters DELCS and DELSCK can be used.

DELCS defines the delay to insert from the activation of the I/O pads to the activation of CS signal (idle2cs) and from the deactivation of CS signal to the deactivation of the I/O pads (cs2idle).

- **DELCS = '000'**: 1 SCK cycles.
- **DELCS = '001'**: 2 SCK cycles.
- **DELCS = '010'**: 4 SCK cycles.
- **DELCS = '011'**: 8 SCK cycles.
- **DELCS = '100'**: 16 SCK cycles.
- **DELCS = '101'**: 32 SCK cycles.
- **DELCS = '110'**: 64 SCK cycles.
- **DELCS = '111'**: 128 SCK cycles.

DELSCK defines the delay to insert from the activation of the CS signal to the start of SCK clock (cs2sck) and from the end of the SCK clock to the deactivation of the CS signal (sck2cs).

- **DELSCK = '000'**: 1 SCK cycles.
- **DELSCK = '001'**: 2 SCK cycles.
- **DELSCK = '010'**: 4 SCK cycles.
- **DELSCK = '011'**: 8 SCK cycles.
- **DELSCK = '100'**: 16 SCK cycles.
- **DELSCK = '101'**: 32 SCK cycles.
- **DELSCK = '110'**: 64 SCK cycles.
- **DELSCK = '111'**: 128 SCK cycles.

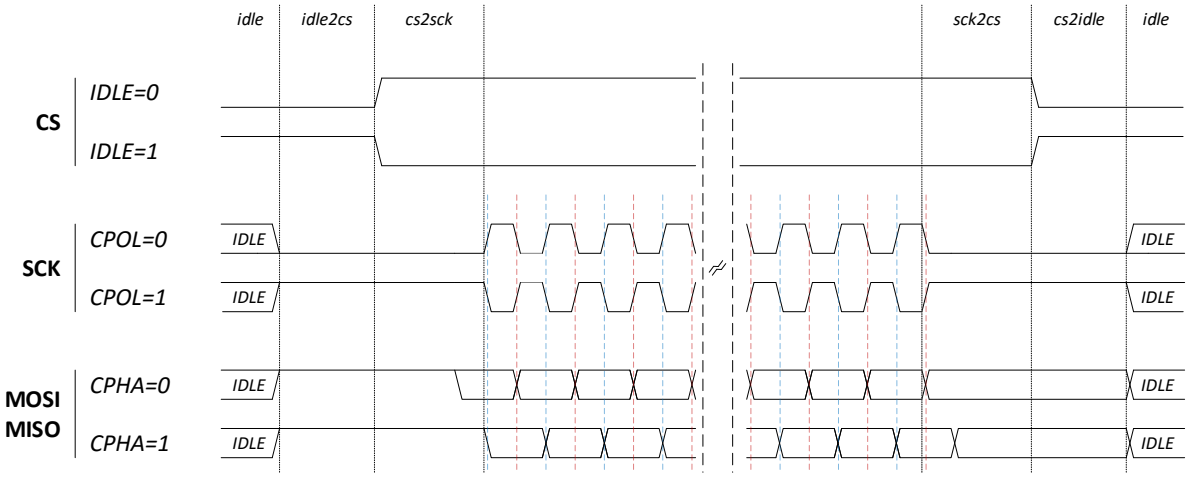


Figure 14: SPI master timing diagram.

SPI data format

Besides defining the SPI operation mode and configuring the desired timings, the input and output data format has to be specified. For the data link from master to slave (MOSI) the data source is provided through the address field targeted inside the User Bank. This value is converted before pushing it to the MOSI pin. During the conversion, the following parameters are used:

The **WSIZE** parameter is used to extend or truncate the received address field to the specified number of bits.

- **WSIZE = '00'**: 8 bits of data after conversion.
- **WSIZE = '01'**: 16 bits of data after conversion.
- **WSIZE = '10'**: 24 bits of data after conversion.
- **WSIZE = '11'**: 32 bits of data after conversion.

The **SWAP** parameter is used to swap the data during conversion.

- **SWAP = '0'**: data to be transmitted through MOSI is calculated based on the received address field. The data is sent as is.
- **SWAP = '1'**: data to be transmitted through MOSI is calculated based on the received address field. The data is swapped prior to sending. When swapping is applied, the LSB of the data to be transmitted through MOSI is sent first.

QoS

ROCKY100 allows Quality of Service (QoS) monitoring of the external devices such as sensors or actuators. Every time an operation is triggered through the SPI the voltage of the load is monitored. The status of the load voltage can be transferred in the answer backscattered to the reader.

In order to enable QoS, the **QOSEN** flag has to be set:

- **QOSEN = '0'**: QoS data is not used.
- **QOSEN = '1'**: QoS data is overlapped to the data received from MISO in the answer backscattered to the reader.

In order to define if the QoS data is attached either at the start of the operation or at the end, the **QOSPOS** flag has to be set to the desired value:

- **QOSPOS = '0'**: If enabled, QoS data is overlapped in the 8 LSB of the backscattered answer.
- **QOSPOS = '1'**: If enabled, QoS data is overlapped in the 8 MSB of the backscattered answer.

The QoS byte includes the following flags:

- **QoS(7)**: VTAG has been above VTAGOFF threshold (0.8V) in the beginning of the transaction.
- **QoS(6)**: VTAG has been above VTAGON threshold (1.4V) in the beginning of the transaction.
- **QoS(5)**: VLOAD has been above VLOADOFF threshold (configured with TRIM_VLOFF) in the beginning of the transaction.
- **QoS(4)**: VLOAD has been above VLOADON threshold (configured with TRIM_VLON) in the beginning of the transaction.
- **QoS(3)**: VTAG has been above VTAGOFF threshold (0.8V) during the complete transaction.
- **QoS(2)**: VTAG has been above VTAGON threshold (1.4V) during the complete transaction.
- **QoS(1)**: VLOAD has been above VLOADOFF threshold (configured with TRIM_VLOFF) during the complete transaction.

- **QoS(0)**: VLOAD has been above VLOADON threshold (configured with TRIM_VLON) during the complete transaction.

QoS Mask

The SPI master can be configured to append or prepend QoS bits in the answer in order to evaluate the validity of the information. Besides attaching the information to the answer, ROCKY100 allows configuring a QoS mask so that, if the QoS value is lower to the specified one, the SPI master will not generate signaling towards the load.

This configuration allows saving energy in cases where the available energy is known to be insufficient for the action of the load.

The QOSMASK byte checks the following conditions:

- **QOSMASK(7-4)**: RFU.
- **QOSMASK(3)**: VTAG has been above VTAGOFF threshold (0.8V) in the beginning of the transaction.
- **QOSMASK(2)**: VTAG has been above VTAGON threshold (1.4V) in the beginning of the transaction.
- **QOSMASK(1)**: VLOAD has been above VLOADOFF threshold (configured with TRIM_VLOFF) in the beginning of the transaction.
- **QOSMASK(0)**: VLOAD has been above VLOADON threshold (configured with TRIM_VLON) in the beginning of the transaction.

SPI MASTER CONTROL

The RFID interface standard allows performing two different operations directed to any memory position: read and write. The read operation allows specifying an address field and the number of words to read and returns the content of the specified number of words to the reader. The write command instead, specifies the address field and the data to write and returns success or error codes, no actual data.

Given that the SPI bridge requires bidirectional data flow and specifying the length of the signaling is a desirable feature, the write command is discarded. The read command is used to control the SPI bridge.

Read Command

The read command specified in the supported RFID protocols includes the following parameters:

- **MemBank**: specifies whether the Read command accesses Reserved, EPC, TID, or User memory.
- **WordPtr**: specifies the starting word address inside MemBank, where words are 16 bits in length.
- **WordCount**: specifies the number of 16-bit words to be read.

Given the memory space definition of ROCKY100, any address starting from CURRENT_SBA inside the User memory bank is mapped to the SPI bridge. The address field uses the Extensible Bit Vectors (EBV) format, and thus has no specified limit on its maximum length. Even though, given the real implementation of RFID systems, most readers limit the length of the address field to a 32bit length variable in their APIs. Under this circumstances, the address field parameter can be used to specify up to 32bits of data from the RFID interface towards the SPI bridge.

In order to share the other devices mapped within the User memory bank, the SPI bridge will only process read operations targeted to address CURRENT_SBA and above. This means that the minimum value of the address field the SPI bridge will ever receive is CURRENT_SBA. As data values from 0x00 to CURRENT_SBA - 1 may be of interest, the address field is converted into MOSI data by subtracting the offset value CURRENT_SBA to the address field. Moreover, in case the reader used in the system has a limited addressing capability, an

SPI_OFFSET value is added to the final output data. The final data value used to output through MOSI is given by:

- **MOSI_DATA** = $WordPtr - CURRENT\_SBA + SPI\_OFFSET$

Besides specifying the data to push through the MOSI pin, the number of SCK cycles to generate has to be defined. For this purpose the WordCount parameter is used. As for each word specified in the WordCount parameter the RFID interface allows returning 16 bits towards the reader, the SPI bridge generates 16 SCK cycles per WordCount unit. The data read in the MISO pin is returned back to the reader as the content of the requested memory locations.

Notes:

- Memory read operations that span between different devices in the user memory bank are not allowed.
- If a read operation to the user memory bank with WordCount=0 is requested, only the address range of the targeted device is considered.

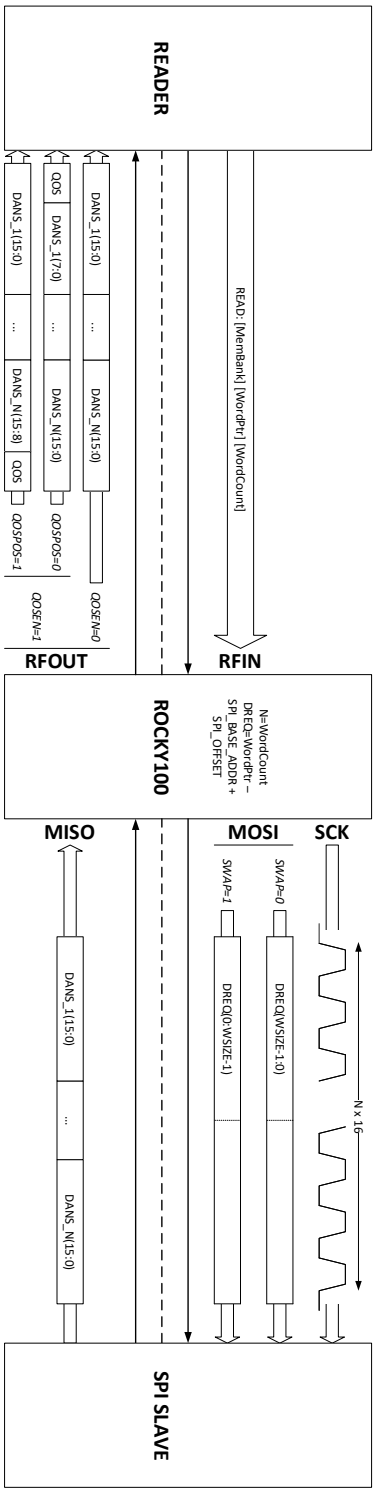


Figure 15: SPI master signaling.

SPI MASTER REGISTERS

SPI_MASTER_CTL

15	14	13	12 11 10	9 8 7	6 5	4 3	2	1	0
IDLE	**CPOL**	**CPHA**	**DELCS**	**DELSCK**	**DIVSCK**	**WSIZE**	**SWAP**	**TRUNC**	**IDLEMOSI**

Memory bank: User

Address: 0x0B

Type: R/W

Factory value: 0x0000

Description: SPI configuration word.

[15] **IDLE:** value of SPI signaling during idle state.

- **'0'**: logic low.
- **'1'**: logic high.

[14] **CPOL:** polarity of SPI signaling.

- **'0'**: SCK starts in logic low.
- **'1'**: SCK starts in logic high.

[13] **CPHA:** phase of SPI signaling.

- **'0'**: Data pushed in even SCK edges.
- **'1'**: Data pushed in odd SCK edges.

[12:10] **DELCS:** delay in SCK cycles before and after CS toggling.

- **'000'**: 1
- **'001'**: 2
- **'010'**: 4
- **'011'**: 8
- **'100'**: 16
- **'101'**: 32
- **'110'**: 64
- **'111'**: 128

[9:7] **DELSCK:** delay in SCK cycles before and after SCK burst.

- **'000'**: 1
- **'001'**: 2
- **'010'**: 4
- **'011'**: 8
- **'100'**: 16
- **'101'**: 32
- **'110'**: 64
- **'111'**: 128

[6:5] **DIVSCK:** Divisor for SCK frequency.

- **'00'**: /1 (f_{SCK} = 1MHz).
- **'01'**: /2 (f_{SCK} = 500kHz).
- **'10'**: /4 (f_{SCK} = 250kHz).
- **'11'**: /8 (f_{SCK} = 125kHz).

[4:3] **WSIZE:** Word size configuration.

- **'00'**: 8 bits.
- **'01'**: 16 bits.
- **'10'**: 24 bits.
- **'11'**: 32 bits.

[2] **SWAP:** Data swap control bit.

- **'0'**: MOSI data is sent MSB first.
- **'1'**: MOSI data is sent LSB first .

[1] **TRUNC:** truncation for non 16bit length words.

- **'0'**: do not truncate.
- **'1'**: truncate SCK cycles.

[1] **IDLEMOSI:** logical value of the MOSI output after the SPI command has been transmitted.

- **'0'**: logic low.
- **'1'**: logic high.

QOS_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU						QOSEN	QOSPOS	QOSMASK							

Memory bank: User

Address: 0x0C

Type: R/W

Factory value: 0x00

Description: QoS control word.

[9] **QOSEN:** QoS mark enable bit for SPI master brigde.

- **'0'**: QoS data is not used.
- **'1'**: QoS data enabled.

[8] **QOSPOS:** QoS mark position configuration bit for SPI master brigde.

- **'0'**: QoS data overlaps the LSB.
- **'1'**: QoS data overlaps the MSB.

[7:0] **QOSMASK:** QoS mask for SPI master brigde.

SPI_OFFSET

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI_OFFSET_H															

Memory bank: User

Address: 0x1C

Type: R/W

Factory value: 0x00

Description: MSB of SPI_OFFSET.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI_OFFSET_L															

Memory bank: User

Address: 0x1D

Type: R/W

Factory value: 0x00

Description: LSB of SPI_OFFSET.

The value specified in SPI_OFFSET is used to convert WordPtr into MOSI_DATA.

SPI SLAVE

ROCKY100 includes a SPI slave in order to share the internal resources with an external SPI master device. This interface is useful to share the same memory from both, C1G2 UHF RFID interface and SPI interface. Moreover, the SPI slave interface can also be used for debug purposes allowing to monitor the internal state machines of the digital processor.

SPI SLAVE CONFIGURATION

The SPI slave integrated in ROCKY100 is configured to work with negative polarity (SCK starts low) and positive phase (data is pushed in positive edges and read in engative edges). The Chip Select (CS) signal is configured to be active in low. The next figure shows the signaling between an external SPI master and the integrated SPI slave.

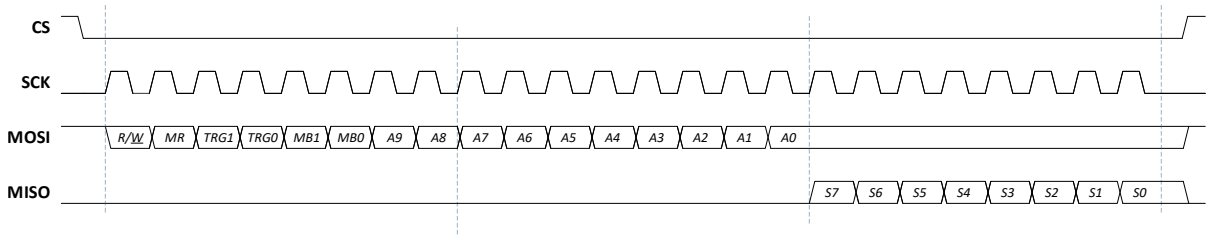


Figure 16: SPI slave signaling.

Parameter	Description
R/$\overline{W}$	Read/Write indicator
MR	Multiple Read indicator
TRG[1:0]	Target memory space
MB[1:0]	Memory Bank
A[9:0]	Address
S[7:0]	Status work

Any command issued by the SPI master shall follow the specified structure. The first bit is the Read/Write indicator. In order to request a read operation, this bit has to be asserted. Otherwise, the command will be treated as a write request.

The second bit indicates if a read operation is supposed to be a single word read or a multiple word read. In order to specify a multiple word read, this bit has to be asserted. This bit has no meaning if the *R/$\overline{W}$* indicator is set to '0'.

The *TRG* field specifies the target memory space for the requested operation. When '00' value is specified, the EPC C1G2 memory space is targeted. This means that exactly the same registers can be accessed from the RF interface and the SPI interface. Note that in this mode, the lock bits set for the C1G2 interface are also effective from the SPI interface. This means that if some memory location has been locked for the RFID interface, the SPI access to these registers will also be restricted.

If the value of *TRG* is set to ’01’, the digital processor status memory space is targeted. This mode supports only read operations.

TRG	Target memory space
’00’	EPC C1G2 memory space
’01’	Digital processor monitoring memory space
’10’	RFU
’11’	RFU

Once the target memory space is defined, the Memory Bank selection bits and Address field specify the targeted register.

MB	Memory Bank
’00’	Reserved
’01’	EPC
’10’	TID
’11’	User

After receiving the first two bytes from the SPI master, the integrated SPI slave evaluates if the requested operation is legal or not. The first byte sent from the SPI slave to the SPI master through the MISO line contains the status word. In case the request can be fulfilled, the status word will contain the acknowledgment value 0xAA. If the request has an invalid format or the request is illegal, the status word will contain the error code 0x81.

SPI SLAVE CONTROL

Single Read

When a single read operation is requested, the SPI master shall keep on generating SCK cycles in order to retrieve the content of the specified register. The content of the requested register is pushed just after the status word in the MISO line.

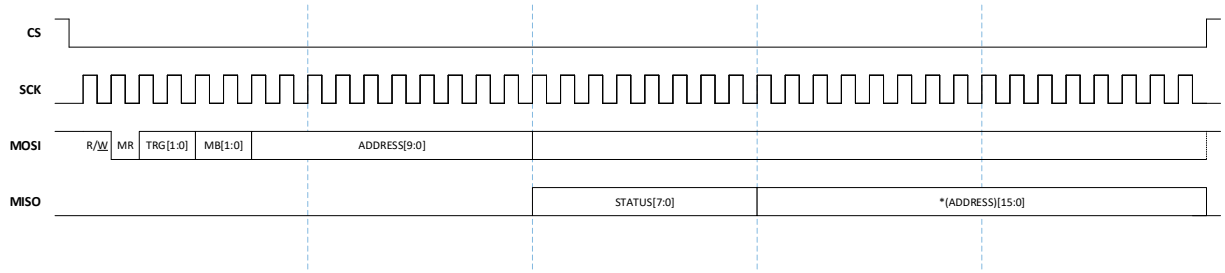


Figure 17: SPI slave single read.

Multiple Read

When a multiple read operation is requested, the SPI master shall keep on generating SCK cycles in order to retrieve the content of the specified register. The content of the requested register is pushed just after the status word in the MISO line as in a single read operation. However, in this case if the SPI master keeps on generating even more SCK cycles, the integrated SPI slave will push the content of the next register through MISO. Every time the content of the current register is read, the address pointer will be incremented automatically.

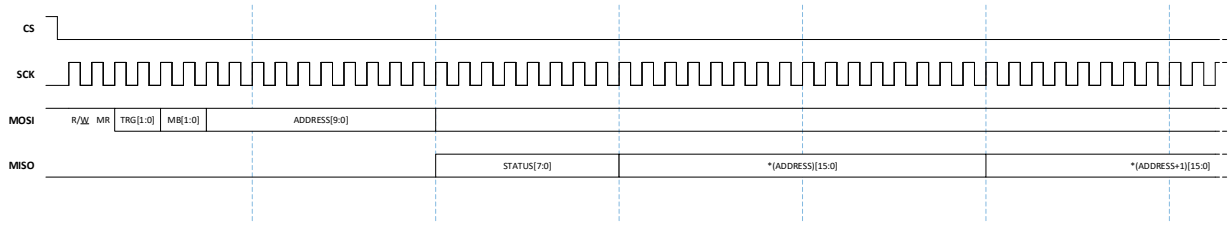


Figure 18: SPI slave multiple read.

Single Write

When a write command is requested, after specifying the address of the register to be written the new content has to be specified. This requires two additional bytes to be sent from the SPI master. The status word acknowledging the operation or notifying an error will be pushed to the MISO line right after receiving the data.

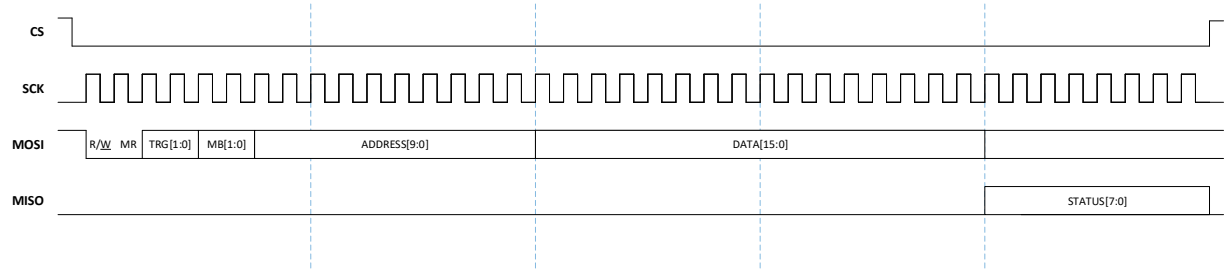


Figure 19: SPI slave write.

EDGE DETECTOR

ROCKY100 includes two instances of the edge detector module. Both of them are functionally equal and can be configured separately.

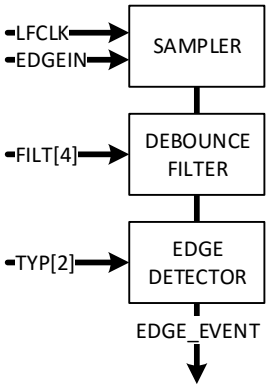


Figure 20: Edge detector block diagram.

SIGNAL MONITORING

The edge detector included in ROCKY100 samples the incoming signal with the LFOSC clock, of about 1 kHz. In order to avoid meta-stability issues, three input flip-flops are used in series adding up a 2 extra cycle latency.

Given the nature of some logic inputs, bouncing may be expected. A configurable debounce filter is included in ROCKY100. The filter will validate a change in the state of the input signal only after receiving a given number of continuous samples with the new value. The depth of the debounce filter can be set up to 128 samples through the FILT parameter of the EDGE_CTL register.

FILT	Debounce filter depth
’000’	1 sample
’001’	2 samples
’010’	4 samples
’011’	8 samples
’100’	16 samples
’101’	32 samples
’110’	64 samples
’111’	128 samples

EDGE DETECTION

The filtered signal is continuously monitored in order to detect state changes. The edge detector can be configured to generate events upon receiving falling edges, rising edges or any of them.

TYP	Edge type
’00’	None
’01’	Falling edges
’10’	Rising edges
’11’	Both

EDGE DETECTOR REGISTERS

EDGE_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU			**FILT_1**			**TYP_1**		**RFU**			**FILT_2**			**TYP_2**	

Memory bank: User

Address: 0x1B

Type: R/W

Factory value: 0x0000

Description: Edge detector control word.

[15:13] RFU

[12:10] **FILT_1:** Debounce filter depth of module 1.

- **'000'**: 1 sample.
- **'001'**: 2 samples.
- **'010'**: 4 samples.
- **'011'**: 8 samples.
- **'100'**: 16 samples.
- **'101'**: 32 samples.
- **'110'**: 64 samples.
- **'111'**: 128 samples.

[9:8] **TYP_1:** Edge type of module 1.

- **'00'**: None.
- **'01'**: Falling edge.
- **'10'**: Rising edge.
- **'11'**: Both.

[7:5] RFU

[4:2] **FILT_2:** Debounce filter depth of module 2.

- **'000'**: 1 sample.
- **'001'**: 2 samples.
- **'010'**: 4 samples.
- **'011'**: 8 samples.
- **'100'**: 16 samples.
- **'101'**: 32 samples.
- **'110'**: 64 samples.
- **'111'**: 128 samples.

[1:0] **TYP_2:** Edge type of module 2.

- **'00'**: None.
- **'01'**: Falling edge.
- **'10'**: Rising edge.
- **'11'**: Both.

EXAMPLE CONFIGURATION

In order to clarify the operation of the edge detector, the following example configuration is presented. In this case the following configuration has been used:

- **FILT**: 2 samples.
- **TYP**: rising edge.

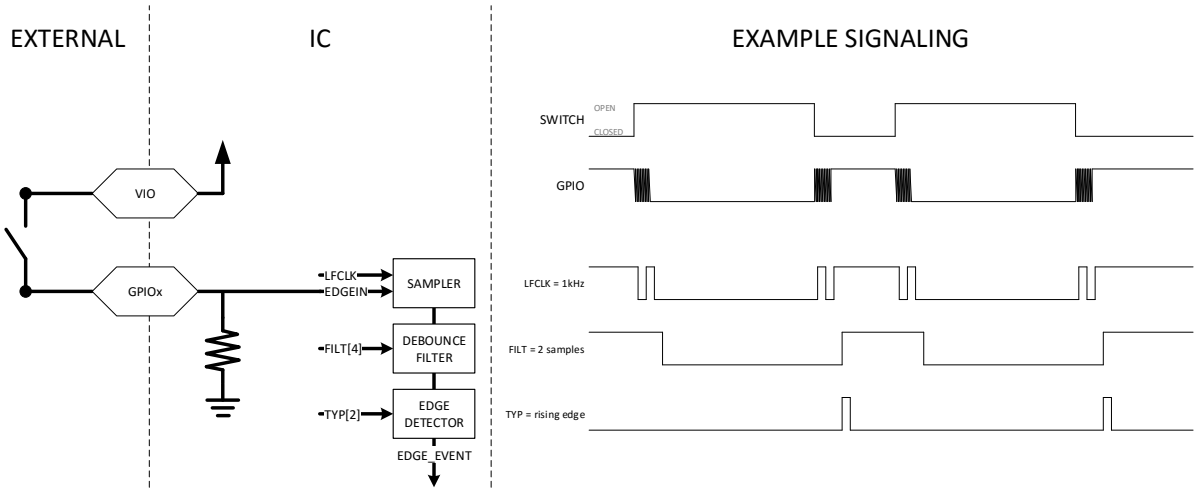


Figure 21: Example edge detector configuration.

EVENT LOGGER

ROCKY100 includes one instance of the event logger module. This module allows to keep track of the number of times an event has occurred. Moreover, it allows storing the time-stamp and the associated data of one of these events. Information of which occurrence to store can be set depending on the value of the time-stamp or the associated data.

The device has to be powered on during the activity of the event logger. However, it is possible to store the logged information in non volatile memory so that the data can be retrieved later on, even if the device has lost power.

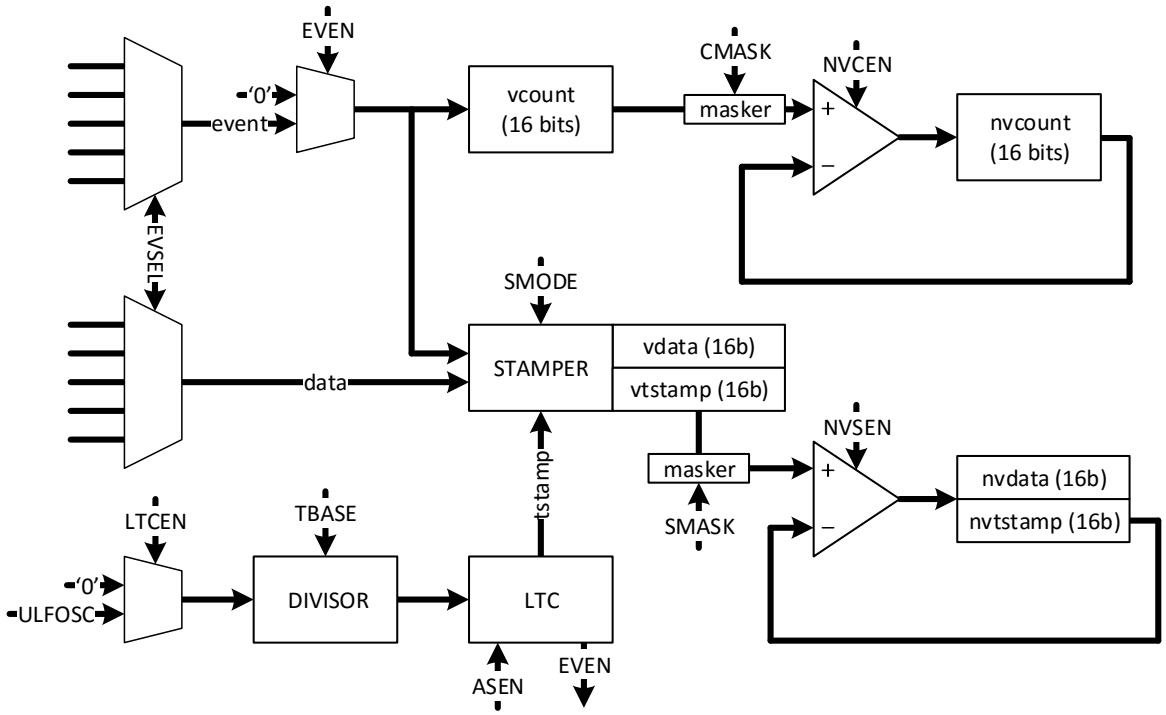


Figure 22: Event logger block diagram.

EVENT COUNTER

The event logger can be triggered from different sources. When enabled, the device keeps track of the number of times the selected event has occurred. This count is stored in the volatile register *vcount*.

It is possible to enable storing the count in the non volatile register *nvcount*. A comparator checks if the content in the volatile and non volatile counter registers is different, and if so, copies the value of the volatile register to the non volatile register. Moreover, as saving data to non volatile memory is more power consuming, it is possible to mask some of the bits of the volatile counter prior to entering the comparator, so that the update from volatile to non volatile memory is done only after a significant increment in the volatile counter.

Table 11: Logger events.

EVSEL	Event	Description
100	EDGE_1	Edge detector 1
101	EDGE_2	Edge detector 2
110	EDGE_1 | EDGE_2	Edge detector 1 or 2
111	EDGE_1 & EDGE_2	Edge detector 1 and 2

LOG TIME COUNTER

In order to keep track of the timeline of the events, the event logger includes a Log Time Counter (LTC) module. This module is driven by the ULFOSC clock of about 1Hz. Notice that this clock is based in an RC circuit, and even if it is trimmed for increased precision, the drift in temperature may be significant.

The LTC stores the value of the timestamp in the 16bit *LTC* volatile register. Depending on the application, the duration of the device usage may exceed 65.535 seconds. For such cases, a time base divisor can be used. This divisor reduces the resolution of the time base, thus allowing keeping track of the events during longer periods of time up to 3 years. The time base is set through the TBASE parameter in the LOG_CTL register.

TBASE	Time base
’000’	1 s
’001’	5 s
’010’	10 s
’011’	30 s
’100’	1 min
’101’	5 mins
’110’	10 mins
’111’	30 mins

EVENT STAMP

Alongside with the event counter log, it is possible to keep track of the time and associated data of one of the event occurrences. In order to configure how the device shall select which occurrence to store, the SMODE parameter has to be set.

SMODE	Event stamp mode
’00’	First occurrence
’01’	Last occurrence
’10’	Occurrence with minimum associated data
’11’	Occurrence with maximum associated data

The time-stamp and associated data of the event is stored in the *vtstamp* and *vdata* volatile registers. It is possible to enable saving the event stamp in the non volatile registers *nvtstamp* and *nvdata*. A comparator checks if the content in the volatile and non volatile time-stamp registers is different, and if so, copies the values of the volatile registers to the non volatile registers. Moreover, as saving data to non volatile memory is more power consuming, it is possible to mask some of the bits of the volatile time-stamp prior to entering the comparator, so that the update from volatile to non volatile memory is done only after a significant increment in the volatile time-stamp.

AUTOSTART

The EVEN flag in the LOG_CTL register enables the configured event to enter the event logger module. In order to start logging an event, this flag has to be set. However, it is also possible to configure the device so that the EVEN flag is set automatically after a certain period of time. For this purpose the LTC block is used. If the ASEN flag is set, the LTC module will automatically set the EVEN flag when an overflow occurs. Thus, introducing a negative value in the LTC sets a start time for the event logger module.

EVENT LOGGER REGISTERS

LOG_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EVSEL			**EVEN**	**NVCEN**	**CMASK**				**SMODE**		**NVSEN**	**SMASK**			

Memory bank: User

Address: 0x21

Type: R/W

Factory value: 0x8000

Description: Event logger module control word.

[15:13] **EVSEL:** Event selector.

- **'100'**: EDGE_1
- **'101'**: EDGE_2
- **'110'**: EDGE_1 | EDGE_2
- **'111'**: EDGE_1 & EDGE_2

[12] **EVEN:** Event logger enable.

- **'0'**: event logger disabled.
- **'1'**: event logger enabled.

[11] **NVCEN:** Non-volatile counter enable.

- **'0'**: non-volatile counter disabled.
- **'1'**: non-volatile counter enabled.

[10-7] **CMASK:** Count mask.

[6-5] **SMODE:** Stamp mode.

- **'00'**: first.
- **'10'**: minimum data.
- **'01'**: last.
- **'11'**: maximum data.

[4] **NVSEN:** Non-volatile stamp enable.

- **'0'**: non-volatile stamp disabled.
- **'1'**: non-volatile stamp enabled.

[3-0] **SMASK:** Stamp mask. Refer to table 7.

LOG_NVCOUNT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOG_NVCOUNT															

Memory bank: User

Address: 0x22

Type: R/W

Factory value: 0x0000

Description: Event logger non-volatile count.

LOG_NVTSTAMP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOG_NVTSTAMP															

Memory bank: User

Address: 0x23

Type: R/W

Factory value: 0x0000

Description: Event logger non-volatile time-stamp.

LOG_NVDATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOG_NVDATA															

Memory bank: User

Address: 0x24

Type: R/W

Factory value: 0x0000

Description: Event logger non-volatile data.

LOG_VCOUNT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOG_VCOUNT															

Memory bank: User

Address: CUR_PBA + 0x03 (Default: 0x83)

Type: R

Factory value: 0x0000

Description: Event logger volatile count.

LOG_VTSTAMP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOG_VTSTAMP															

Memory bank: User

Address: CUR_PBA + 0x04 (Default: 0x84)

Type: R

Factory value: 0x0000

Description: Event logger volatile time-stamp.

LOG_VDATA

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOG_VDATA															

Memory bank: User

Address: CUR_PBA + 0x05 (Default: 0x85)

Type: R

Factory value: 0x0000

Description: Event logger volatile data.

LTC_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU											LTCEN	TBASE			ASEN

Memory bank: User

Address: 0x1E

Type: R/W

Factory value: 0x00

Description: Log Time Counter control word.

[4] **LTCEN:** Log Time Counter enable.

- **'0'**: LTC disabled.
- **'1'**: LTC enabled.

[3:1] **TBASE:** Time base.

- **'000'**: 1 sec
- **'001'**: 5 secs
- **'010'**: 10 secs
- **'011'**: 30 secs
- **'100'**: 1 min
- **'101'**: 5 mins
- **'110'**: 10 mins
- **'111'**: 30 mins

[0] **ASEN:** Auto Start enable.

- **'0'**: auto-start disabled.
- **'1'**: auto-start enabled.

LTC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTC															

Memory bank: User

Address: CUR_PBA + 0x02 (Default: 0x82)

Type: R/W

Factory value: 0x0000

Description: LTC counter.

PWM

ROCKY100 contains a programmable PWM waveform generator. The output of this module can be bypassed to any GPIO and can also be used to control the GLOADSW. The PWM module included in ROCKY100 allows configuring the IDLE state, the time in ON, the time in OFF and the number of cycles to generate. In case the number of cycles to generate is set to 0, the PWM module will continuously generate the signaling.

In order to trigger the signaling, there are two options. If the device should start automatically after startup, the AUTO_START bit can be set in the configuration. Otherwise, any *Write* operation with non-zero data towards the PWM_TRIGGER register will trigger the signaling. In case the signaling is configured to continuous generation, it can be stopped sending a *Write* operation with zero data towards the PWM_TRIGGER register.

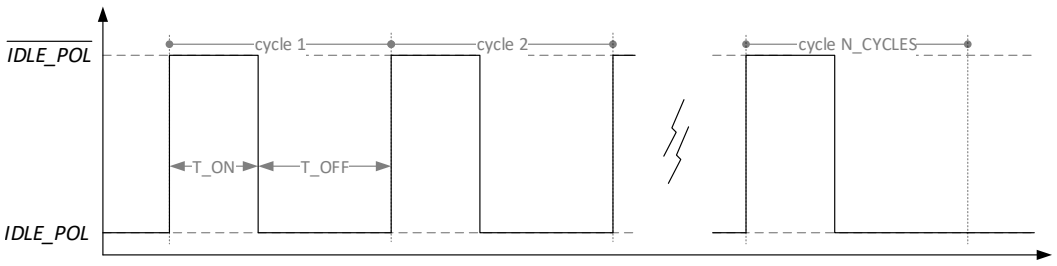


Figure 23: PWM module output waveform.

PWM REGISTERS

PWM_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDLE_POL	**AUTO_START**	**T_ON_IDX**				**T_OFF_IDX**				**N_CYCLES**					

Memory bank: User

Address: 0x25

Type: R/W

Factory value: 0x0000

Description: PWM configuration register.

[15] **IDLE_POL** Logic value of the PWM signal during idle or T_OFF state.

- **'0'**: Logic low.
- **'1'**: Logic high.

[14] **AUTO_START** Forces a continuous PWM signal generation once the tag is powered on.

- **'0'**: Auto start disabled.
- **'1'**: Auto start enabled.

[13-10] **T_ON_IDX** Width of the T_ON pulse.

- $T_{ON}[ms] = 2^{T\_ON\_IDX}$.

[9-6] **T_OFF_IDX** Width of the T_OFF pulse.

- $T_{OFF}[ms] = 2^{T\_OFF\_IDX}$.

[5-0] **N_CYCLES** Number of T_ON - T_OFF cycles that occur before the peripheral idles.

- **'0'**: Continuous generation.
- **'Others'**: specified number.

PWM_TRIGGER

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PWM_TRIGGER															

Memory bank: User

Address: CURRENT_PBA + 0x11 (Default: 0x91)

Type: W

Factory value: 0x00

Description: PWM waveform trigger.

CONFIGURATION CONTROL

ROCKY100 offers flexible configuration of the integrated devices. This allows the designer to develop customized products depending on the application. However, once the product has been configured, it may be dangerous to leave the configuration registers unprotected because the end user could modify them and alter the characteristics of the device.

In order to prevent unwanted usage of the ROCKY100 powered devices, a configuration lockage mechanism is implemented. ROCKY100 contains three configuration blockage registers labelled from CFG_LOCK_0 to CFG_LOCK_2. There is one of such registers per configuration block in the configuration portion of the user memory bank, and each configuration blockage register allows locking the values of the registers of its configuration block. The configuration blockage registers are located at the beginning of each configuration block. When then *i*th bit of CFG_LOCK_x is set to '1', then the *i*th registers of configuration block *x* is locked. Similarly, when the *i*th bit of CFG_LOCK_x is set to '0', the *i*th registers of configuration block *x* is unlocked. This locking mechanism operates in addition to the permalocks provided by the RFID protocol.

Notice that even the CFG_LOCK_x registers themselves can be locked, so that the lock flags can no longer be modified. For security reasons, it is recommended to lock the meaningful registers as well as the CFG_LOCK_x registers prior to delivering the product to the end user.

In the other hand, the high configurability of ROCKY100 makes its startup slower and more energy consuming as many configuration registers have to be loaded. This is undesired if the end product is not going to make use of all the peripherals in ROCKY100 . Thus, ROCKY100 also provides a mechanism that prevents loading the value of certain configuration registers during startup. For this purpose, two registers exist that indicate which configuration should be loaded and which should be skipped. These registers are labelled CFG_READ_1 and CFG_READ_2 and are associated with configuration blocks 1 and 2 respectively. Each CFG_READ_x register is located at the beginning of its configuration block. Note that there is not a CFG_READ_0 register, as the configuration block 0 is always loaded.

CFG_READ_x operates similarly to CFG_LOCK_x. When the *i*th bit of CFG_READ_x is set to '1' the *i*th register of configuration block *x* is loaded, and when the *i*th bit of CFG_READ_x is set to '0' the *i*th register of configuration block *x* is skipped. Note that ROCKY100 will always load the values of CFG_LOCK_x and CFG_READ_x no matter the current configuration of CFG_READ_1 and CFG_READ_2.

CONFIGURATION CONTROL REGISTERS

CFG_LOCK_0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I0F	**I0E**	**I0D**	**I0C**	**I0B**	**I0A**	**I09**	**I08**	**I07**	**I06**	**I05**	**I04**	**I03**	**I02**	**I01**	**I00**

Memory bank: User

Address: 0x0F

Type: R/W

Factory value: 0x0002

Description: Configuration blockage register.

[15] **I0F:** lock flag for register (0xF) CFG_LOCK_0.

[14] **I0E:** lock flag for register (0xE) SPI_BASE_ADDR.

[13] **I0D:** lock flag for register (0xD) PER_BASE_ADDR.

[12] **I0C:** lock flag for register (0xC) QOS_CTL.

[11] **I0B:** lock flag for register (0xB) SPI_MASTER_CTL.

[10] **I0A:** lock flag for register (0xA) GPIO4_CTL.

[9] **I09:** lock flag for register (0x9) GPIO3_CTL.

[8] **I08:** lock flag for register (0x8) GPIO2_CTL.

[7] **I07:** lock flag for register (0x7) GPIO1_CTL.

[6] **I06:** lock flag for register (0x6) GPIO0_CTL.

[5] **I05:** lock flag for register (0x5) TRIM_VLREGL.

[4] **I04:** lock flag for register (0x4) TRIM_VLOFF.

[3] **I03:** lock flag for register (0x3) TRIM_VLON.

[2] **I02:** lock flag for register (0x2) PSM_CTL.

[1] **I01:** lock flag for register (0x1) TRIM_C1G2OSC.

[0] **I00:** lock flag for register (0x0) OPMODE_CTL_NV.

CFG_LOCK_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I1F	**I1E**	**I1D**	**I1C**	**I1B**	**I1A**	**I19**	**I18**	**I17**	**I16**	**I15**	**I14**	**I13**	**I12**	**I11**	**I10**

Memory bank: User

Address: 0x1F

Type: R/W

Factory value: 0x03FE

Description: Configuration blockage register.

[15] **I1F:** lock flag for register (0xF) CFG_LOCK_1 .

[14] **I1E:** lock flag for register (0xE) LTC_CTL.

[13] **I1D:** lock flag for register (0xD) SPI_OFFSET_L.

[12] **I1C:** lock flag for register (0xC) SPI_OFFSET_H.

[11] **I1B:** lock flag for register (0xB) EDGE_CTL.

[10] **I1A:** lock flag for register (0xA) WDT_CTL.

[9] **I19:** lock flag for register (0x9) RFU.

[8] **I18:** lock flag for register (0x8) RFU.

[7] **I17:** lock flag for register (0x7) RFU.

[6] **I16:** lock flag for register (0x6) RFU.

[5] **I15:** lock flag for register (0x5) RFU.

[4] **I14:** lock flag for register (0x4) RFU.

[3] **I13:** lock flag for register (0x3) RFU.

[2] **I12:** lock flag for register (0x2) RFU.

[1] **I11:** lock flag for register (0x1) TRIM_ULFOSC.

[0] **I10:** lock flag for register (0x0) CFG_READ_1.

CFG_LOCK_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I2F	**I2E**	**I2D**	**I2C**	**I2B**	**I2A**	**I29**	**I28**	**I27**	**I26**	**I25**	**I24**	**I23**	**I22**	**I21**	**I20**

Memory bank: User

Address: 0x2F

Type: R/W

Factory value: 0x7FC0

Description: Configuration blockage register.

[15] **I2F:** lock flag for register (0xF) CFG_LOCK_2 .

[14] **I2E:** lock flag for register (0xE) RFU.

[13] **I2D:** lock flag for register (0xD) RFU.

[12] **I2C:** lock flag for register (0xC) RFU.

[11] **I2B:** lock flag for register (0xB) RFU.

[10] **I2A:** lock flag for register (0xA) RFU.

[9] **I29:** lock flag for register (0x9) RFU.

[8] **I28:** lock flag for register (0x8) RFU.

[7] **I27:** lock flag for register (0x7) RFU.

[6] **I26:** lock flag for register (0x6) RFU.

[5] **I25:** lock flag for register (0x5) PWM_CTL.

[4] **I24:** lock flag for register (0x4) LOG_NVDATA.

[3] **I23:** lock flag for register (0x3) LOG_NVTSTAMP.

[2] **I22:** lock flag for register (0x2) LOG_NVCOUNT.

[1] **I21:** lock flag for register (0x1) LOG_CTL.

[0] **I20:** lock flag for register (0x0) CFG_READ_2.

CFG_READ_1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
r1F	**r1E**	**r1D**	**r1C**	**r1B**	**r1A**	**r19**	**r18**	**r17**	**r16**	**r15**	**r14**	**r13**	**r12**	**r11**	**r10**

Memory bank: User

Address: 0x10

Type: R/W

Factory value: 0xFC0F.

Description: Configuration load register.

[15] **r1F:** no effect.

[14] **r1E:** configuration read flag for register (0xE) LTC_CTL.

[13] **r1D:** configuration read for register (0xD) SPI_OFFSET_L.

[12] **r1C:** configuration read for register (0xC) SPI_OFFSET_H.

[11] **r1B:** configuration read for register (0xB) EDGE_CTL.

[10] **r1A:** configuration read for register (0xA) WDT_CTL.

[9] **r19:** configuration read flag for register (0x9) RFU.

[8] **r18:** configuration read flag for register (0x8) RFU.

[7] **r17:** configuration read flag for register (0x7) RFU.

[6] **r16:** configuration read flag for register (0x6) RFU.

[5] **r15:** configuration read flag for register (0x5) RFU.

[4] **r14:** configuration read flag for register (0x4) RFU.

[3] **r13:** configuration read flag for register (0x3) RFU.

[2] **r12:** configuration read flag for register (0x2) RFU.

[1] **r11:** configuration read flag for register (0x1) TRIM_ULFOSC.

[0] **r10:** no effect.

CFG_READ_2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
r2F	**r2E**	**r2D**	**r2C**	**r2B**	**r2A**	**r29**	**r28**	**r27**	**r26**	**r25**	**r24**	**r23**	**r22**	**r21**	**r20**

Memory bank: User

Address: 0x20

Type: R/W

Factory value: 0x803F.

Description: Configuration blockage register.

[15] **r2F:** no effect.

[14] **r2E:** configuration read flag for register (0xE) RFU.

[13] **r2D:** configuration read flag for register (0xD) RFU.

[12] **r2C:** configuration read flag for register (0xC) RFU.

[11] **r2B:** configuration read flag for register (0xB) RFU.

[10] **r2A:** configuration read flag for register (0xA) RFU.

[9] **r29:** configuration read flag for register (0x9) RFU.

[8] **r28:** configuration read flag for register (0x8) RFU.

[7] **r27:** configuration read flag for register (0x7) RFU.

[6] **r26:** configuration read flag for register (0x6) RFU.

[5] **r25:** configuration read flag for register (0x5) PWM_CTL.

[4] **r24:** configuration read flag for register (0x4) LOG_NVDATA.

[3] **r23:** configuration read flag for register (0x3) LOG_NVTSTAMP.

[2] **r22:** configuration read flag for register (0x2) LOG_NVCOUNT.

[1] **r21:** configuration read flag for register (0x1) LOG_CTL.

[0] **r20:** no effect.

REBOOT

The changes to the configuration of the different devices of ROCKY100 do not apply automatically. The configurations are loaded during the start-up of the device. Thus, after setting new configuration parameters it is necessary to reboot the system in order to load the new configuration.

When dealing with passive systems, the device will reset every time the reader stops emitting power. However, when operating in BAP configuration, the system will not reboot until the battery drains out. It is necessary to trigger a soft-reboot in order to apply the changes in the configuration.

For that purpose, the REBOOT register is included in ROCKY100. Any write command directed to this register will trigger a soft-reboot of the device.

REBOOT REGISTER

REBOOT

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REBOOT															

Memory bank:	User
Address:	CURRENT_PBA + 0x00 (Default: 0x80)
Type:	W
Factory value:	0x00
Description:	Soft-reboot trigger.

WATCHDOG TIMER

ROCKY100 contains a collection of watchdog timers that can be configured to control the reset process of specific sections of the digital core. Each watchdog can be individually enabled or disabled. A global enable flag validates the individual watchdog enable flags, so deasserting this flag disables all watchdogs in the system.

WATCHDOG TIMER REGISTERS

WDT_CTL

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RFU									CTLW	C1G2W	MEMW	RFU_0	LOGW	SPIW	GLOBALW

Memory bank: User

Address: 0x1D

Type: R/W

Factory value: 0x007F

Description: Watchdog enable flags.

[6] **CTLW** Enables the watchdog of the digital core control logic.

- **'0'**: Disabled.
- **'1'**: Enabled.

[5] **C1G2W** Enables the C1G2 core watchdog.

- **'0'**: Disabled.
- **'1'**: Enabled.

[4] **MEMW** Enables the memory address translator watchdog.

- **'0'**: Disabled.
- **'1'**: Enabled.

[3] **RFU_0** Reserved for future use.

[2] **LOGW** Enables the data logger watchdog.

- **'0'**: Disabled.
- **'1'**: Enabled.

[1] **SPIW** Enables the slave SPI logic watchdog.

- **'0'**: Disabled.
- **'1'**: Enabled.

[0] **GLOBALW** Global enable for all watchdogs.

- **'0'**: Disabled.
- **'1'**: Enabled.

APPLICATIONS, IMPLEMENTATION, AND LAYOUT

APPLICATION INFORMATION

The RF pins of ROCKY100 have to be connected to a matched differential antenna. In order to obtain a good performance a matching network has to be included to adapt the impedance of the antenna to the impedance of the tag. It is possible to avoid additional matching components if a custom antenna design with matched impedance is used.

With no more external components, the IC will act as a standard identification tag responding to standard EPC C1G2 readers.

ROCKY100 can also be connected to an external system. In this configuration, the IC can be used either to add an RFID communication bridge to an externally powered circuit or to power up a complete low power external system.

In the BAP configuration the external system is powered by a battery. The IC can be configured to enhance RFID communication range by increasing its power consumption or to leave the battery unconnected to the internal RFID circuitry reducing the leakage current driven from the battery.

In order to operate with external systems in a fully passive configuration, some considerations have to be taken into account. The first one is to ensure that the average current consumption of the external load is in the order of several μA. For an average current consumption beyond 10μA, the maximum communication distance of the system decreases significantly.

Moreover, depending on the power consumption profile of the sensor, additional circuitry may be required. Some sensors have a high power consumption during the start-up of the device. This may cause oscillation in the start-up process of ROCKY100. In order to prevent this behavior, the integrated start-up circuitry has to be configured to keep the sensor shut down during the start up process.

Additionally, even if the average power consumption of the sensor is low, the peak current consumption during measurement has to be evaluated. In order to support high current peaks, an external capacitor may be included.

Once the ROCKY100 has been connected to a matched antenna and to an external system with the correct start up configuration, a reader may singulate the tag and request the data contained in registers mapped to the SPI interface. The tag then executes the SPI communication and backscatters the retrieved data in the answer towards the reader.

In addition to the RF power harvesting and RFID to SPI communication bridge functionality, ROCKY100 can be configured to generate events or to bypass the signals of the UHF RFID front-end. This feature can be of interest to wake-up sleeping external systems using an RFID reader. Different sources to trigger the events can be selected in order to take advantage of the integrated C1G2 processor. For example, the selective anti-collision algorithm defined in the C1G2 standard can be used to wake-up a sub-set of devices powered by ROCKY100.

MECHANICAL, PACKAGING, AND ORDERABLE INFORMATION

REFERENCES

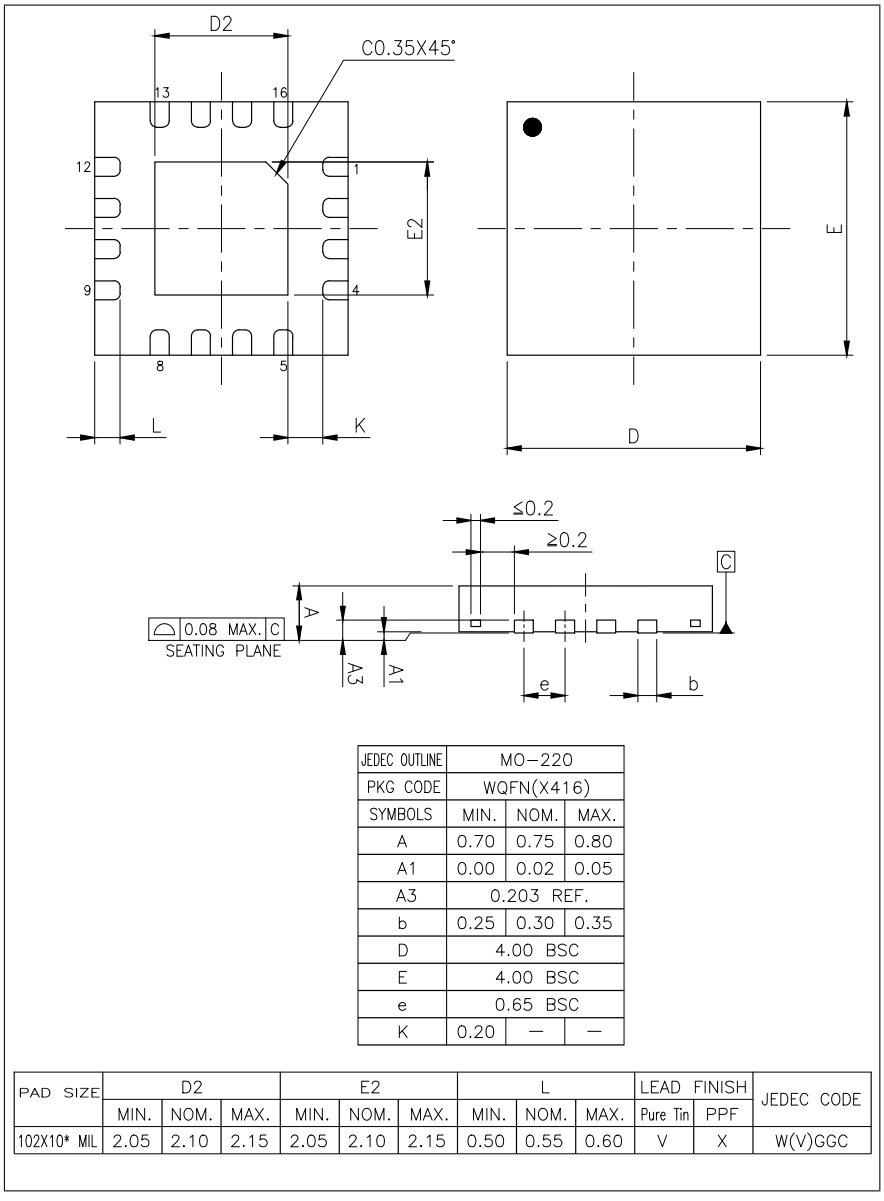
The next table shows the available references of the ROCKY100.

Ref.	Name	Remarks	Status[1]	Package
39316	R100Q16	ROCKY100 IC	PREVIEW	QF16

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: Farsens has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but Farsens does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: Farsens has discontinued the production of the device.

PACKAGING

PACKAGE DESCRIPTION (QF16)

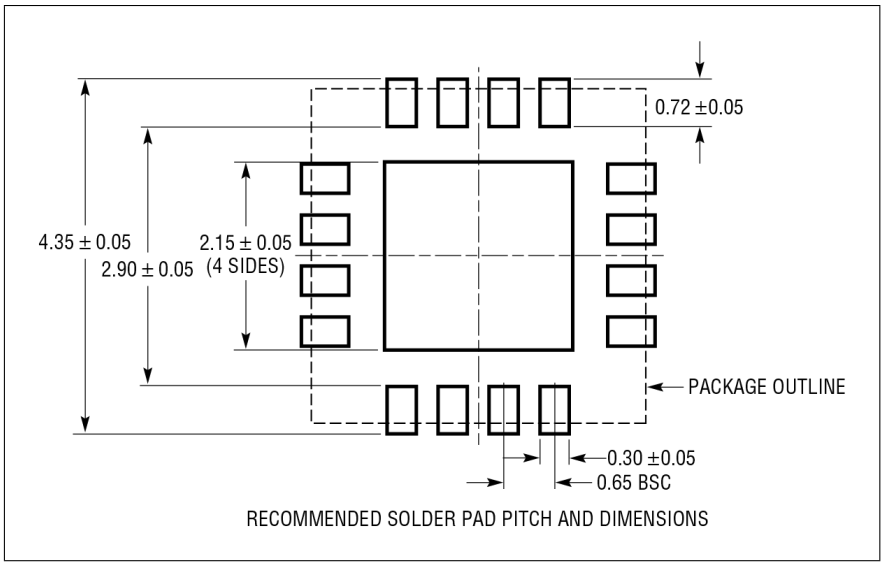


JEDEC OUTLINE	MO–220		
PKG CODE	WQFN(X416)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.25	0.30	0.35
D	4.00 BSC		
E	4.00 BSC		
e	0.65 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
102X10* MIL	2.05	2.10	2.15	2.05	2.10	2.15	0.50	0.55	0.60	V	X	W(V)GGC

Notes: 1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

RECOMMENDED LAND PATTERN (QF16)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

Notes: 1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.